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THE USAFA/8086 - A STATE OF THE ART MICROPROCESSOR SYSTEM. VOLU--ETC(U)

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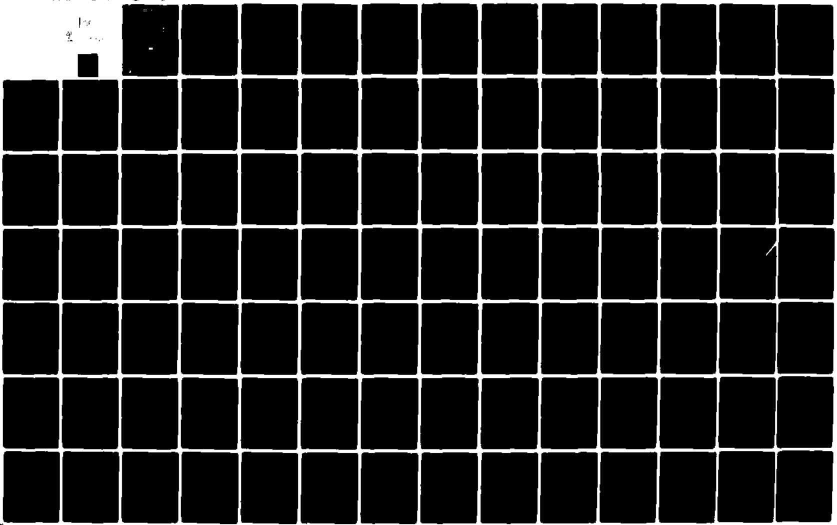

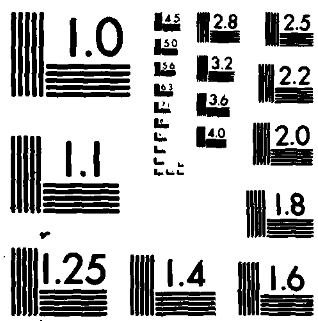

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THE USAFA/8086

A STATE OF THE ART MICROPROCESSOR SYSTEM

VOL. I. SYSTEM HARDWARE

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JUNE 1980

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This research report is presented as a competent treatment of the subject, worthy of publication. The United States Air Force Academy vouches for the quality of the research, without necessarily endorsing the opinions and conclusions of the author.

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This final technical engineering report details the research and development of a modern sixteen bit microprocessor based computer system. The system utilizes state-of-the-art devices to implement many functions often found only in mini-computers and other larger systems. The research detailed in this report was performed under the joint sponsorship of the Air Force Flight Dynamics Laboratory (WPAFB, OH) and the Frank J. Seiler Research Laboratory (USAFA, CO) from August 1978 to March 1980.

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ABSTRACT

This final technical engineering report details the research and development of a modern sixteen bit microprocessor based computer system. The system uses state-of-the-art devices for many functions often found only in minicomputers and other larger systems. The research was performed under the joint sponsorship of the Air Force Flight Dynamics Laboratory (WPAFB, OH) and the Frank J. Seiler Research Laboratory (USAFA, CO) from August 1978 to March 1980.

INTRODUCTION

This report details the research and development of a sixteen bit microprocessor (8086) based computer system. Research was performed at the United States Air Force Academy by the faculty of the Department of Electrical Engineering and members of the cadet wing. The names of individuals associated with this project appear in Appendix B. The purpose of this report is to describe the technical aspects of the developed hardware for engineering and maintenance personnel.

DESIGN GOALS

The original goal of this project was to develop a microprocessor-based application-oriented computer system for the Air Force Flight Dynamics Laboratory (AFFDL) at the Air Force Flight Control Development Laboratory to control a Redifon(1) terrain board type image projection system used in engineering flight simulation. This task immediately placed some engineering demands on the system:

1. High speed, high throughput
2. Floating point arithmetic capable
3. Hybrid capable at the $\pm$ 100 volt level
4. User programmable with minimum difficulty using a High Order Language and a separate Micro Development System
5. User interfaced to allow real time program modification
6. Expandable to allow eventual stand alone programming capability
7. Direct memory accessible to allow high speed interface to other simulation computers

Coordination with the F.J. Seiler Research Laboratory (FJSRL), located at the U.S. Air Force Academy, revealed they also had a desire to develop a microcomputer-based system which pushed the state-of-the-art in this area. The exact application area of the FJSRL was missile guidance systems.

This project was thus jointly funded by these two organizations. Contact at AFFDL was Mr. James Eicher. The associated project number was 24030115. Contact for FJSRL was LtCol Joseph S. Ford under Project 2304F264.

The Microcomputer System

The microcomputer system was built in a modular manner with overall system design and specific engineering guidance provided as necessary by the author. Figure 1 shows a block diagram of the overall system. Each of the succeeding chapters details the blocks of Figure 1.

Each of the chapters of this report leans heavily upon technical data written or accumulated by the individuals credited in Appendix B.

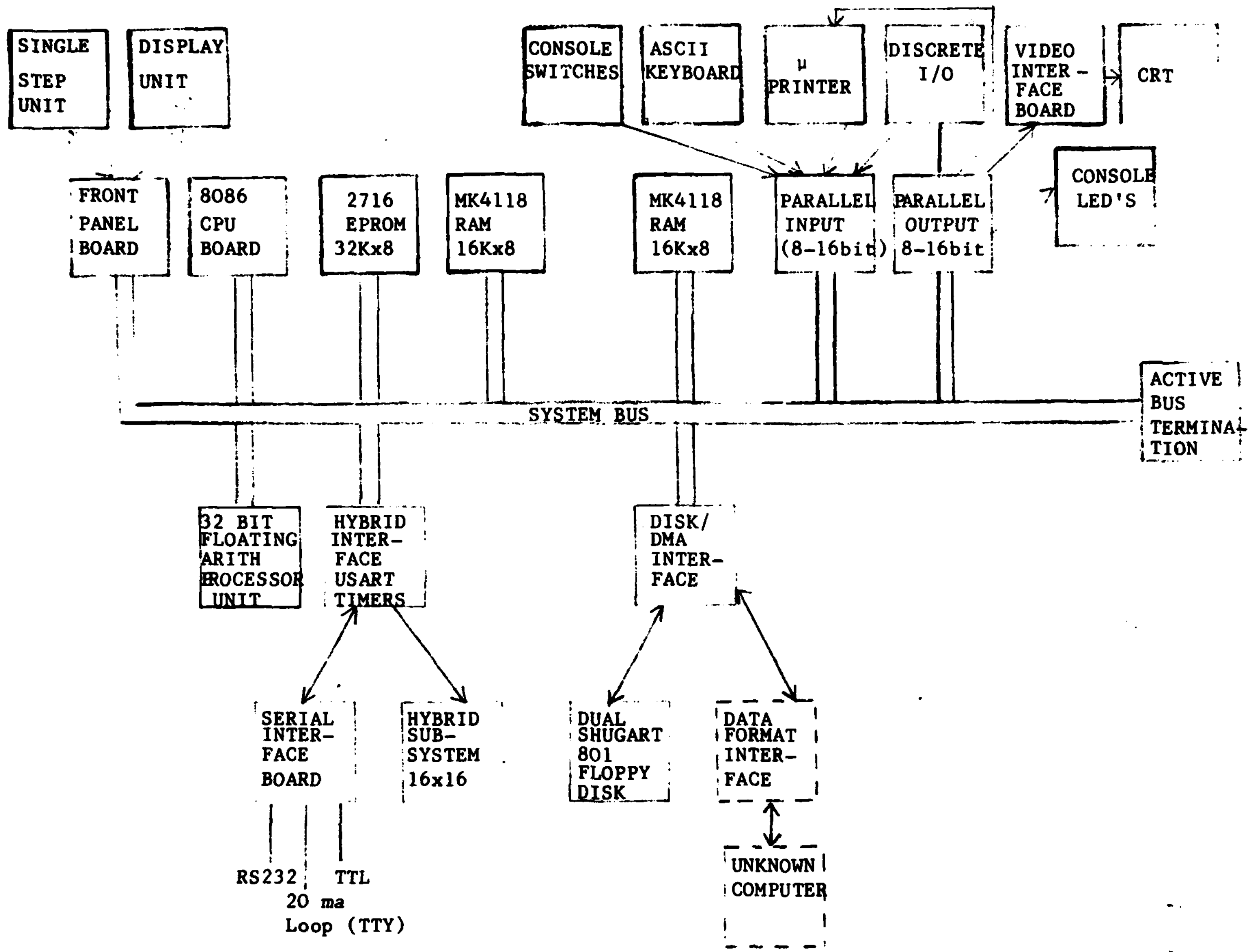


FIGURE 1. USAFA/8086 BLOCK DIAGRAM

I. THE COMPUTER BUS SYSTEM AC/DC POWER DISTRIBUTION AND SYSTEM CONFIGURATION

This chapter details computer power and signal distribution as well as the basic system configuration. The following specific areas are discussed:

1. Computer Signal Distribution
   a. Card Slot Assignment
   b. I/O Port Assignment
2. DC Power Distribution
3. AC Power Distribution

Computer Signal Distribution

To facilitate signal distribution, an S-100 hardware bus system was chosen for use with this system. Although the S-100 hardware was used, the electrical signal distribution is not S-100 compatible nor was it ever intended to be. At the time of the original bus design (Aug 78) and even as of the writing of this report no 16 bit processor compatible bus system has been accepted by industry or professional societies. Each manufacturer, rather, prefers to enhance the development of its own subsystems and thus no consensus is universally attainable.

Table 1 shows the signal distribution used in this system. The primary motives in signal placement were:

1. Convenience of card design
2. Noise immunity
3. Maximum system flexibility

Although not fully used, this system has a full 20 bit (1M Byte) address bus along with the 16 bit data bus. To avoid complicated space-consuming redundant demultiplexing on each card these signals are demultiplexed

TABLE 1. 8086 SYSTEM BUS STANDARD

1	+5	26	$\overline{\text{S0}}$	51	+5	76	SP
2	+12	27	$\overline{\text{S1}}$	52	-12	77	$\overline{\text{MRDC}}$
3	RDY1	28	$\overline{\text{S2}}$	53	SP	78	$\overline{\text{IORC}}$
4	IR0	29	SROM	54	$\overline{\text{EXT}}$ $\overline{\text{CLR}}$	79	A19 (MSB)
5	IR1	30	A18	55	INH1	80	A17
6	IR2	31	A16	56	$\overline{\text{SEL5}}$	81	A15
7	IR3	32	A14	57	DRQ3	82	A13
8	IR4	33	A12	58	$\overline{\text{DACK3}}$	83	A11
9	IR5	34	A10	59	SP	84	A9
10	IR6	35	A8	60	SP	85	A7
11	IR7	36	A6	61	SP	86	A5
12	RDY2	37	A4	62	SP	87	A3
13	$\overline{\text{AEN1}}$	38	A2	63	DRQ2	88	A1
14	$\overline{\text{AEN2}}$	39	A0 (LSB)	64	$\overline{\text{DACK2}}$	89	D15 (MSB)
15	NMI	40	D14	65	$\overline{\text{AIOWC}}$	90	D13
16	SP	41	D12	66	$\overline{\text{AMWC}}$	91	D11
17	$\overline{\text{HLDA}}$	42	D10	67	$\overline{\text{IOWC}}$	92	D9
18	$\overline{\text{HLDR}}$	43	D8	68	$\overline{\text{MWTC}}$	93	D7
19	$\overline{\text{TEST}}$	44	D6	69	PS	94	D5
20	QS1	45	D4	70	PROT	95	D3
21	QS0	46	D2	71	UNPROT	96	D1
22	$\overline{\text{LOCK}}$	47	D0 (LSB)	72	SP	97	$\overline{\text{INTA}}$
23	SP	48	GND	73	ALE	98	CLK (4 MHz)
24	SP	49	PCLK (2 MHz)	74	$\overline{\text{BHE}}$	99	POC
25	SP	50	GND	75	RESET (OUT)	100	GND

SP1, SP2, SP3 are spares

PS, PROT, UNPROT, INH1, INH2 are memory control signals

POC $\Longrightarrow$ Power on Clear

prior to placement on the bus. The signals AØ and DØ represent the least significant bits of the address and data buses respectively. Signals which are overscored (i.e., $\overline{\text{HLDA}}$) are active low.

The bus is actively terminated using the methodology employed by the manufacturer of the 11 slot motherboard which was one of the few items in the system procured commercially (2). Figure 1 shows the basic termination circuit used.

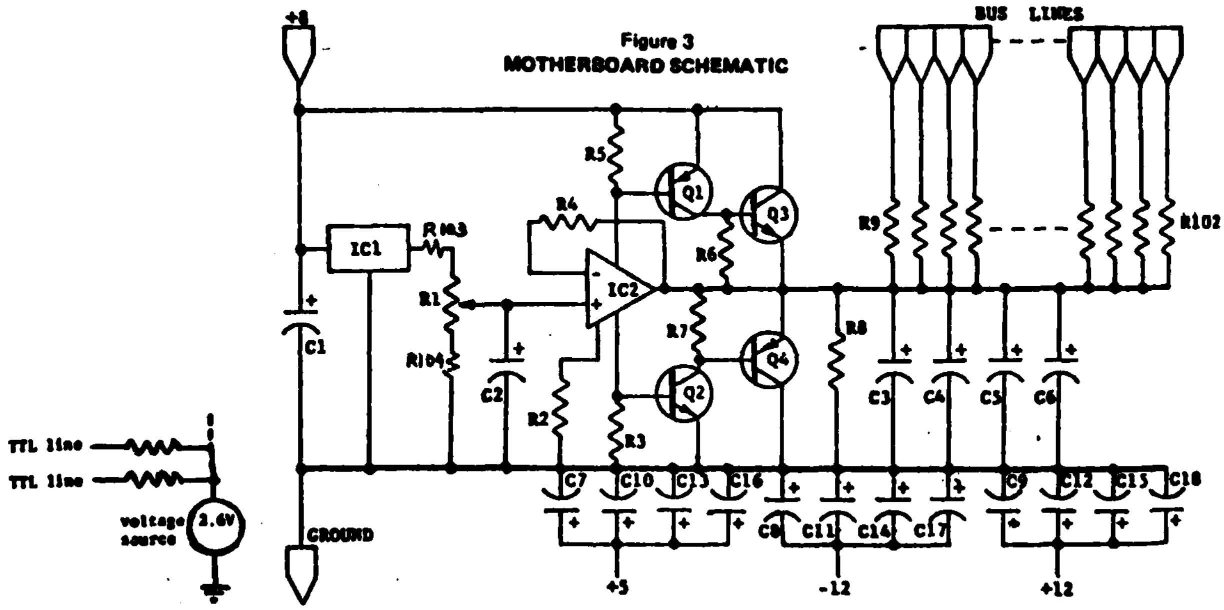


FIGURE 2. BUS TERMINATION CIRCUIT

Card Slot Assignment

The cards in the system will physically fit in the system only in one direction, thus providing protection against human error during card insertion. The motherboard in the system is a true bus; that is each card may be placed in any slot and expected to function properly although slots will be assigned for convenience of signal distribution from the cards to external locations. The following slot assignments are made in the USAFA/8086 Computer System:

TABLE 2. CARD SLOT ASSIGNMENTS - USAFA/8086

SLOT	CARD
1 (Farthest left from the front)	Front Panel Controller
2	NOT USED
3	RAM-1 (00000H to 03FFFH)
4	CPU
5	APU and Controller
6	RAM-2 (040000H to 08000H)
7	EPROM (F8000 to FFFFFH)
8	Hybrid Interface
9	DMA/Floppy Disk Interface
10	Parallel Output ($F\emptyset_H$ to FF_H)
11	Parallel Input ($F\emptyset_H$ to FF_H)

The serial interface, special 28 volt I/O, and Video interface cards do not require motherboard slots as signals are exchanged over cabling to cards installed in the motherboard.

I/O Port Assignments

Although the 8086 will support I/O operations to up to 65, 536 (2^{16}) devices only 8 address lines (A7 to AØ) are decoded for I/O applications within this system. Table 3 specifies those I/O ports currently assigned for use in the system.

TABLE 3. I/O PORT ASSIGNMENTS

(All port addresses are given in base 16)

All ports not otherwise indicated are available for system expansion.

I/O PORT	USAGE
00 and 02	Interrupt Controller (8259A)
10, 12, 14	AM9511 APU/Controller
21, 23	Serial I/O (8251A)
31, 33, 35, 37	Timers (8253)
40 - 5F (16 bit)	Hybrid Subsystem
60 - 7F (16 bit)	Hybrid Subsystem Expansion
CØ,C2,C4,C6,C8,CA,CC,CE	Disk Controller (WD-1791)
C1,C3,C5,C7,C9,CB,CD,CF	DMA Controller
FØ - FF	Parallel Input/Output

DC Power Distribution

Regulated power is distributed to the main computer system from a 5 volt 25a supply as well as a separate ±15v supply.

Figure 3a shows the basic concept of DC power distribution within the main computer system.

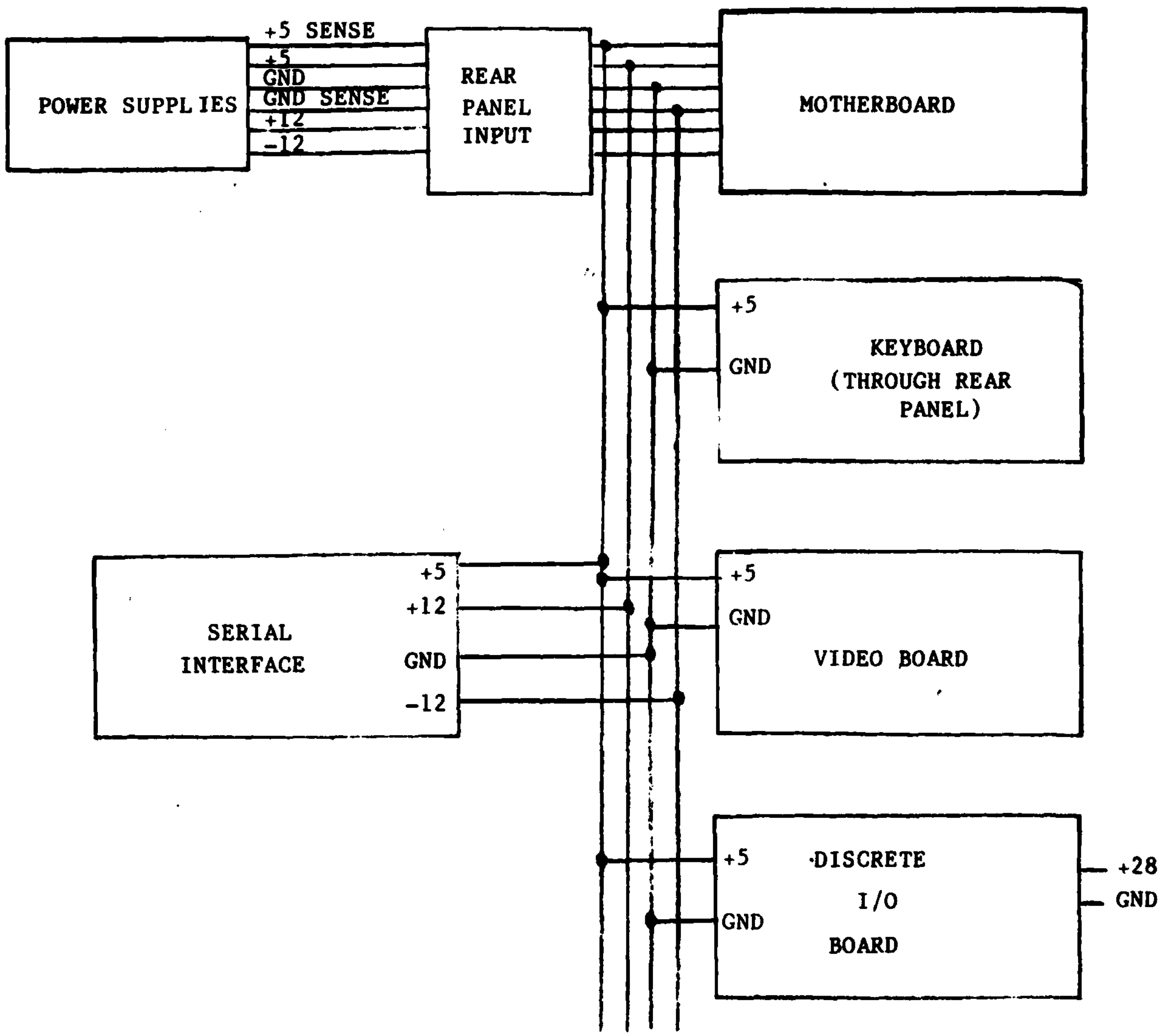


FIGURE 3a. DC POWER DISTRIBUTION - MAIN SYSTEM

The following color code is used for DC Power Distribution within the system to the extent possible:

+5	Yellow
+12	Red
-12	Green
GND	Black
Sense	Striped

Primary power distribution is made using #16 AWG stranded wire. The primary of the DC supply is fused at the supply. Additional 5 volt filtering is supplied by a 3600 µfd capacitor located at the motherboard.

The DC power supply should never be operated without a load attached to the sense lines since this leads to immediate failure of the LM723 regulators employed by the system.

The hybrid subsystem employs its own DC supply to provide as much isolation as possible between the analog and digital portions of the system for noise suppression. Figure 3b shows the DC power distribution at the sub bus.

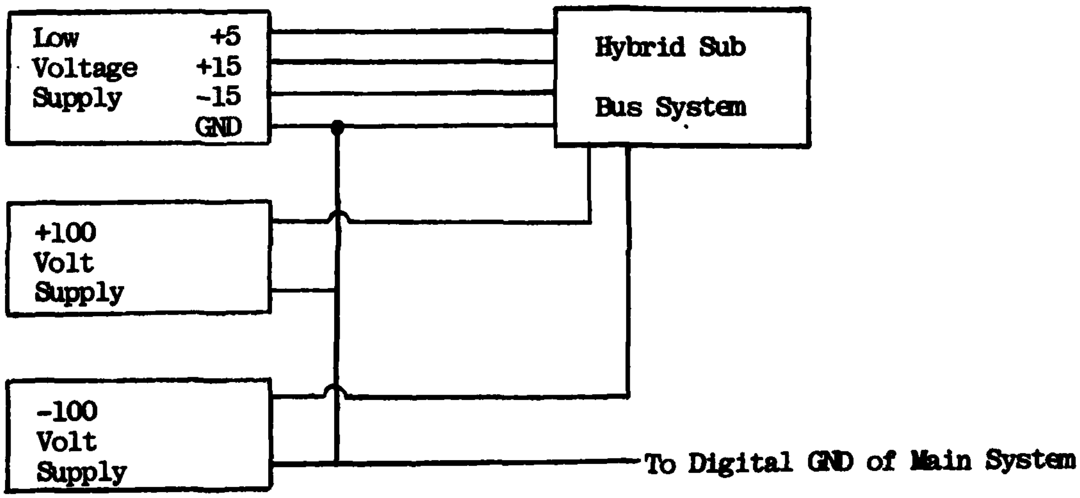


FIGURE 3b. DC POWER DISTRIBUTION - HYBRID SYSTEM

The low voltage supply is manufactured by Deltron, Inc. system[3]. The ±100 volt supplies were manufactured by Power/Mate Corporation and have the following specifications[4]:

Output Voltage:	+5,±15	±100
Line Regulation:	.02%	.075%
Output Regulation:	.05%	.075%
Ripple:	.01% rms	5.0mv p-p max

These high voltage supplies are potentially lethal and extreme caution is necessary while working in their vicinity. Under no circumstances should any card on the hybrid sub-bus be removed while power is applied. This will lead to damage to equipment and extreme hazard to personnel.

At delivery the system DC Power supplies were set as follows:

TABLE 4. POWER SUPPLY VOLTAGE SETTING

	NOMINAL SETTING	ACTUAL SETTING
Main Computer	5 Volt	5.00
	+12	+11.92
	-12	-12.24
Hybrid Sub Bus	+110	+109.3
	-110	-110.5
	+5	+5.02
	+15	+15.05
	-15	-15.04

Although desirable it should not be necessary to have these exact settings since system components tolerate ±5% minimum deviation in supply voltage.

AC Power Distribution

AC Power distribution is provided from the main computer back panel. Outlets are provided for the system CRT, μ Printer, hybrid supplies, and disk subsystem. As viewed from the rear of the computer, Figure 4 shows the normal AC assignments with the right most outlet required to be the main computer +5 volt DC voltage supply.

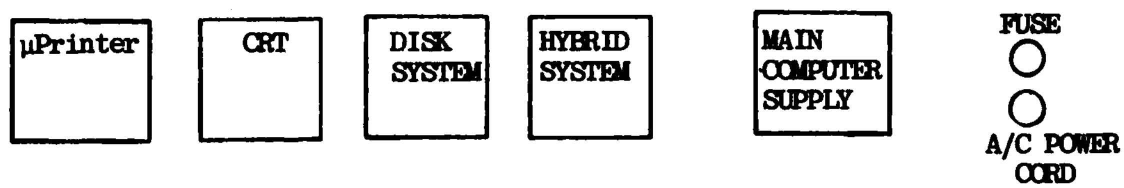


FIGURE 4. AC POWER OUTLETS

Figure 5 schematically shows the method of A/C Power Distribution.

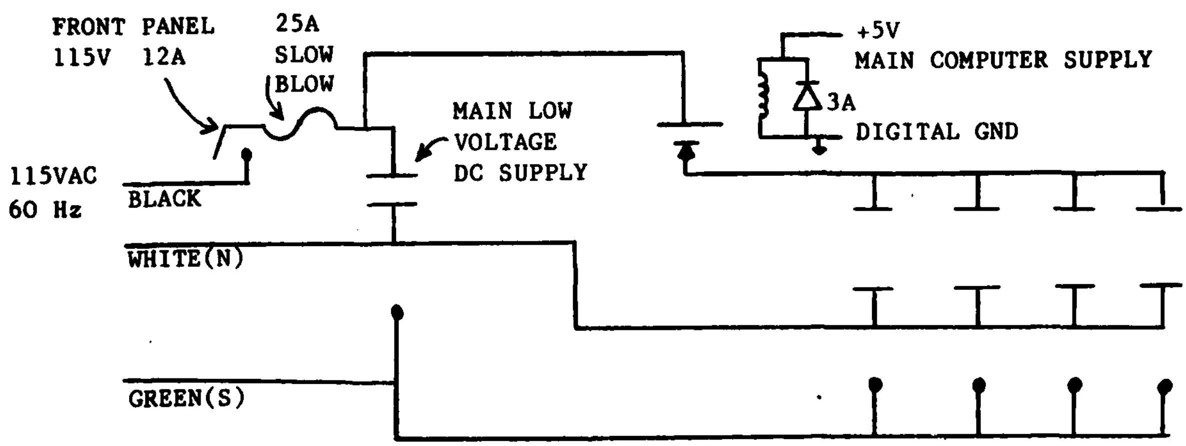


FIGURE 5. AC POWER WIRING

The initial A/C transient is large, necessitating the slow blow fuse in the main AC line.

The system works as follows. AC Power is supplied through the switch on the front panel to the main low voltage DC supply. This supply through its +5 volt output then energizes a relay whose contacts are rated at 25A steady state and 160A surge. The diode prevents a reverse voltage surge when the relay is de-energized.

II. THE FRONT PANEL CIRCUITRY

The front panel circuitry consists of two main wirewrapped circuit boards. These are the switch/led/signal interface and the address/data/control/single step unit.

<u>Switch/Led/Signal Interface</u>

The switches used on the front panel are of the double pole single throw type. They only needed to be single pole but parts available were used. The poles are wired in parallel as shown in Figure 6.

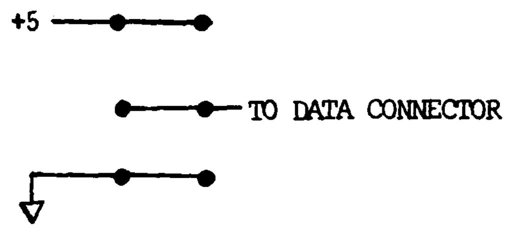


FIGURE 6. TYPICAL FRONT PANEL SWITCH

A small capacitor is placed between the switches on the power lines to suppress noise generation. The switches are connected by a sixteen pin cable to the input port used. The pinout of the cable is shown in Figure 7. The cable is connected to input ports FE and FF_H.

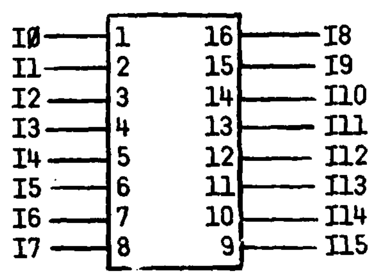


FIGURE 7. SWITCH CABLE PINOUT

The leds have their anode connected to V_{CC} (5 volts) and are of the self limiting type with internal resistor. Figure 8 shows the connection of the led. Figure 9 shows the cabling connection to output ports FE_H and FF_H. Note that these ports are of the inverting type to allow proper operation of the leds. Ports FE_H and FF_H use 8283 inverting output ports.

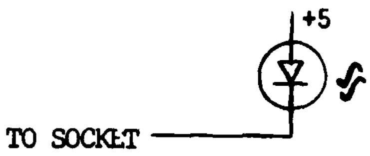


FIGURE 8. LED CIRCUIT

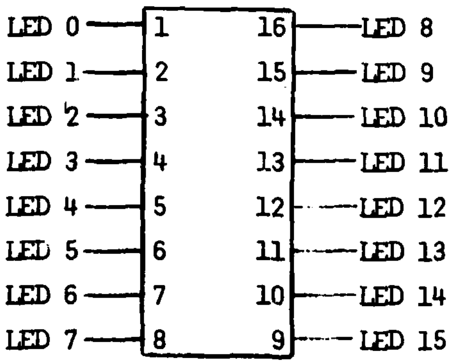


FIGURE 9. LED CABLING CONNECTOR

The following signals are used on the front panel and are cabled as shown in Figure 10. The other end of the control cable is connected to the Front panel Controller Board.

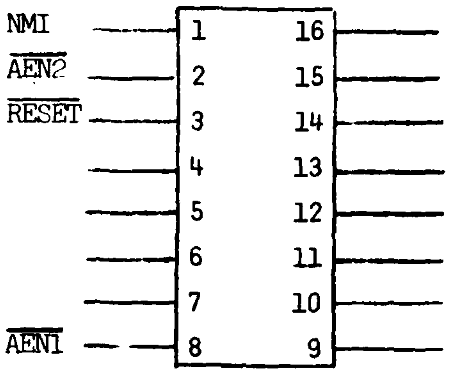


FIGURE 10. CONTROL SIGNAL CABLING

The $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ lines are used by the SINGLE STEP/RUN switch as shown in Figure 18 of Chapter III. The $\overline{\text{NMI}}$ line is connected to the NMI pushbutton switch as shown in Figure 11. The reset line is connected similarly.

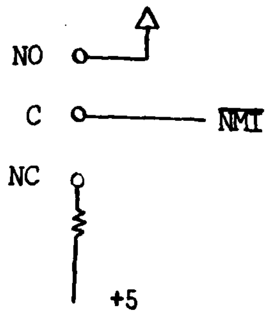


FIGURE 11. NMI PUSHBUTTON SWITCH

As you look at the front panel, the displays are numbered as shown in Figure 12.

#1	#2	#3	#4	#5
	#6	#7	#8	#9

FIGURE 12. DISPLAY NUMBERING

The control signals are presented through discrete leds as shown in Figure 13.

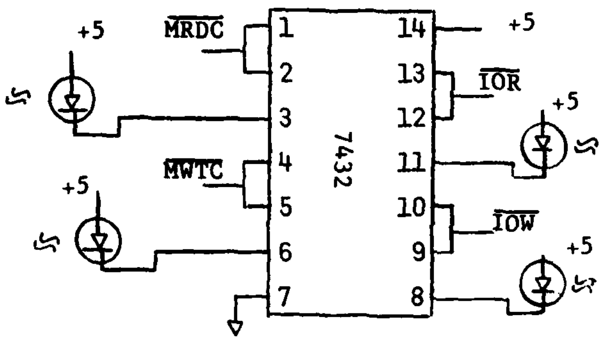


FIGURE 13. DISPLAY OF CONTROL LINES

The most complicated part of the display board is the single step controller. Its operation is as follows. One half of a 7474 presettable D flip flop is used to drive a discrete transistor (2N2222) which is connected to the RDY2 line. The CPU issues the ALE signal every cycle. This signal is used to cause the flip flop to be set driving the RDY2 line low and stopping the CPU. When the user pushes the STEP pushbutton, its output is debounced and applied to the clock input of the flip flop. The rising edge causes the flip flop to reset since the D input is grounded and the RDY2 line is high until the next ALE signal occurs (1 machine cycle). The circuitry used is shown in Figure 14.

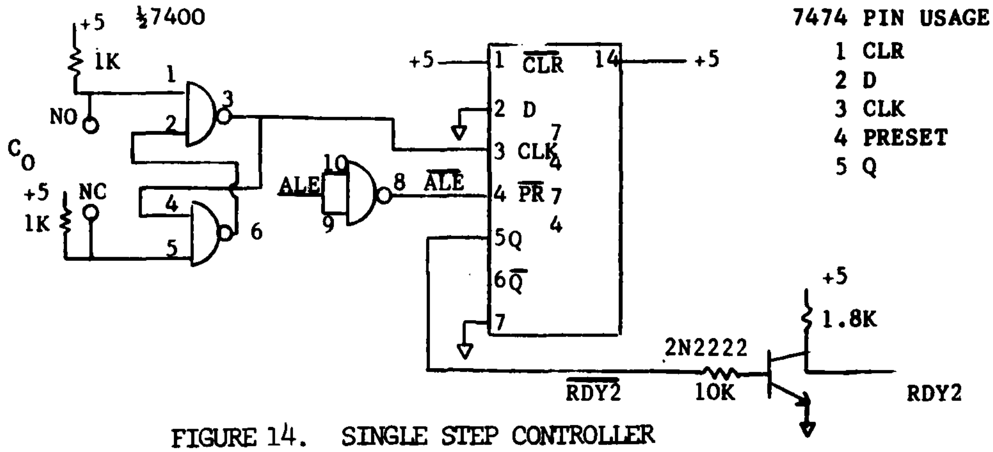


FIGURE 14. SINGLE STEP CONTROLLER

To interconnect the single step controller/display we need 20 address lines, 16 data lines, 6 control lines, clock and signal ground. These signals are provided by a 40 pin connector and a 16 pin connector. The pinouts for these connectors are shown in Figure 15. The cables connect to the Front Panel Controller board described in the next chapter.

40 PIN CONNECTOR

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40
$\overline{IOW}$	$\overline{MWTC}$	$\overline{RDY2}$	PCLK	A8	A9	A10	A11	A12	A13	A14	A15	AØ	A1	A2	A3	A4	A5	A6	A7
GND	$\overline{IOR}$	$\overline{MRDC}$	ALE	D8	D9	D10	D11	D12	D13	D14	D15	DØ	D1	D2	D3	D4	D5	D6	D7
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39

16 PIN CONNECTOR

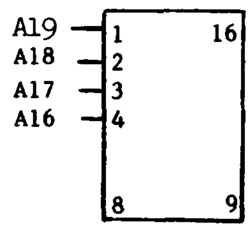


FIGURE 15. CONNECTOR PINOUTS, SINGLE STEP CONTROLLER

The Single Step/Address/Data/Control Display

When the USAFA/8086 is placed in the single step mode of operation the single step unit provides a static visual readout using 9 seven segment (FND 503) displays. The control lines MEMR, MEMW, IOR, and IOW are also displayed. When the 8086 is in the run mode the display also provides useful information as the operator becomes accustomed to seeing a certain dynamic pattern when the system is executing his program.

The Seven Segment Displays

The address and data busses are connected similarly to drive the MOS Signetics 9368 latch/hex decoder which in turn provides data to FND 503 display as shown in Figure 16.

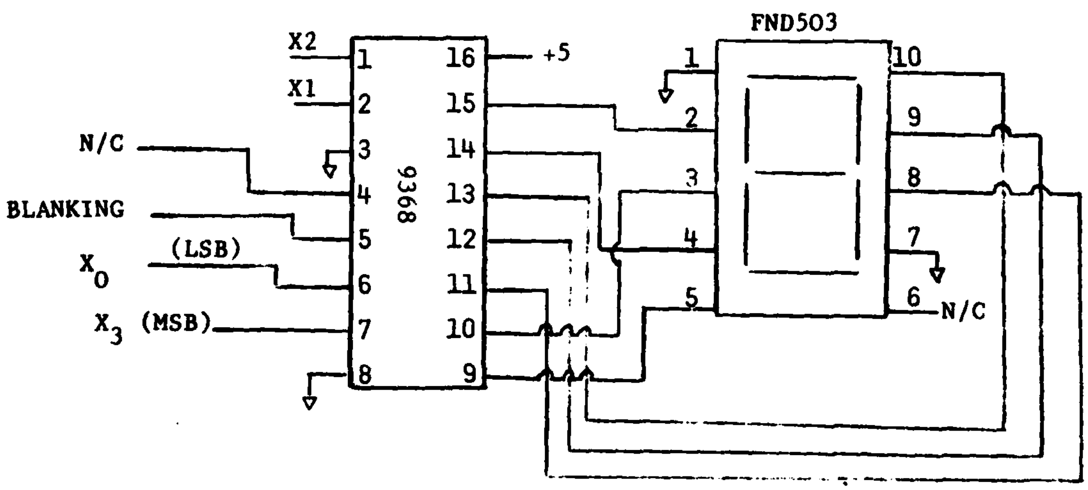


FIGURE 16. DECODER/DISPLAY CONFIGURATION

The displays are blanked 50% of the time using the 2MHz clock from the system bus to conserve power. The system, however, is not multiplexed and actually uses nine separate decoder drivers. The Fairchild 9368 is described in (5). The FND503 is a common cathode display which the 9368 sources current to light the appropriate segments to form the hexadecimal characters. Table 5 shows the connections required from the data bus for each of the nine displays.

TABLE 5. DISPLAY CONNECTIONS

DISPLAY	XØ	X1	X2	X3
1	A16	A17	A18	A19
2	A12	A13	A14	A15
3	A8	A9	A1Ø	A11
4	A4	A5	A6	A7
5	AØ	A1	A2	A3
6	D12	D13	D14	D15
7	D8	D9	D1Ø	D11
8	D4	D5	D6	D7
9	DØ	D1	D2	D3

III. THE FRONT PANEL CONTROLLER BOARD

The front panel controller board consists of the interface to the front panel including both display and control cabling as well as miscellaneous timing circuits required by other boards in the system. Figure 19 shows the physical layout of the board.

The Display/Control Interface

The 40 pin connector which is described in Figure 15 in Chapter II connects directly the required signals to their appropriate pin on the bus as described in Table 1 of Chapter I. The remaining four address lines A19-A16 are brought to the display board through 16 pin connector #2. The pinout for this connector is shown below in Figure 17.

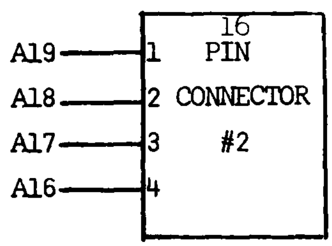


FIGURE 17 . UPPER ADDRESS LINE CABLING

The control cabling to the front panel is connected to 16 pin connector #1. The connector is shown in Figure 18 .

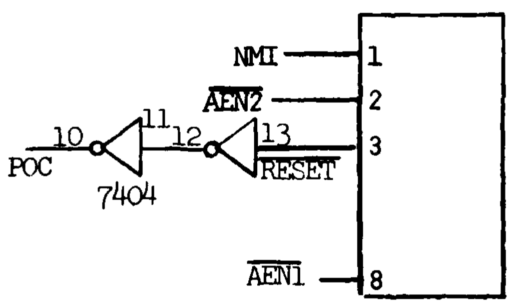


FIGURE 18. FRONT PANEL CONTROL CABLING

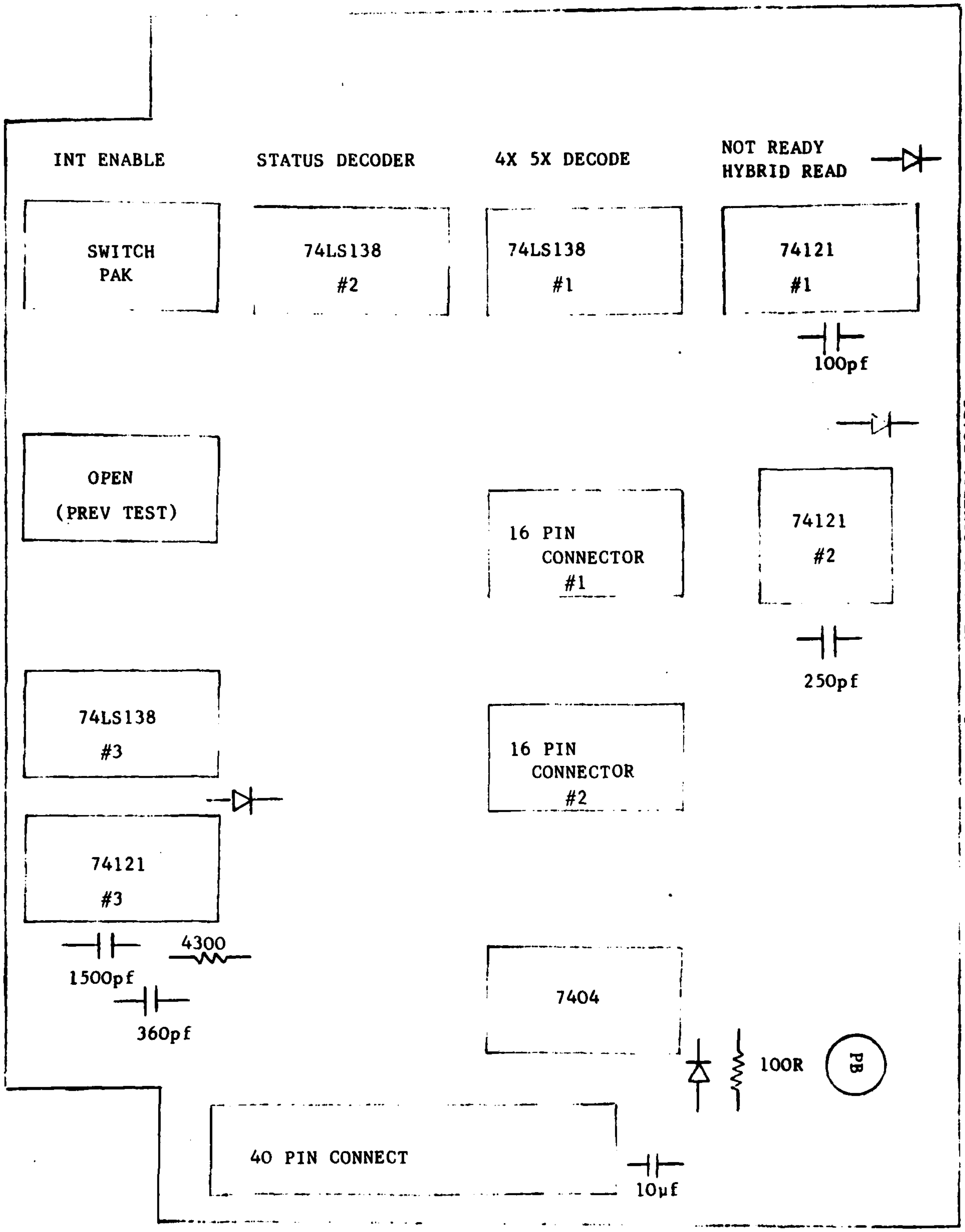


FIGURE 19. FRONT PANEL CONTROL BOARD

The power on clear/reset circuit is contained in the upper right hand corner of the board. A switch is located there which is parallel to the front panel switch allowing either to reset the system. Since this signal must be transmitted on the system bus it is double buffered prior to transmission.

<u>Timing Circuitry</u>

The signals provided by the 8228 controller such as $\overline{MRDC}$, $\overline{IORC}$, etc. are not provided in adequate time for use with system ready circuits. To alleviate this problem the CPU status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ were decoded as shown in Figure 20 .

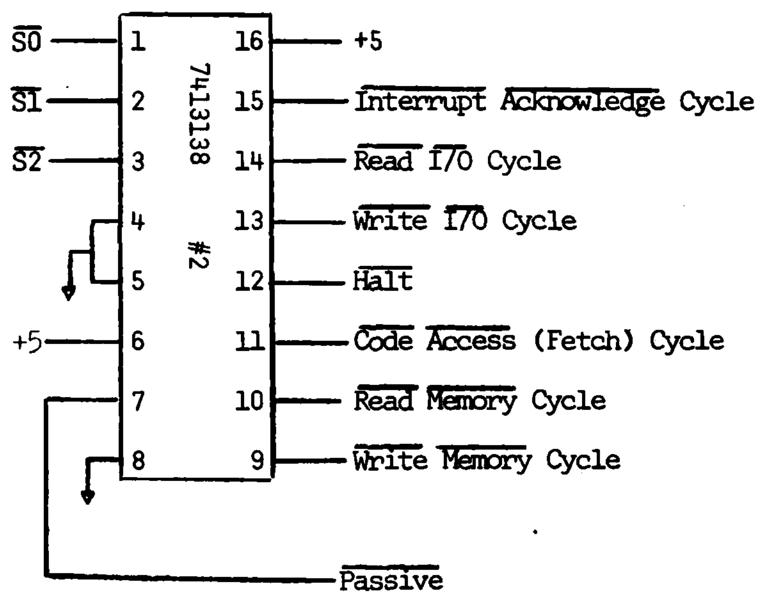


FIGURE 20. STATUS DECODER

In particular, it is necessary to allow several of the circuits additional time during the I/O Read process. Since the Arithmetic Processor Unit is constrained to run at 2MHz, all reads must first allow this processor time to see the request and secondly, time to provide the requested data. A similar problem exists for the reading of the hybrid input channels since the hybrid system controller must be allowed to finish his current task prior to relinquishing the hybrid systems cache memory. The circuitry used to insert the required "not ready" period for the APU is shown in Figure 21.

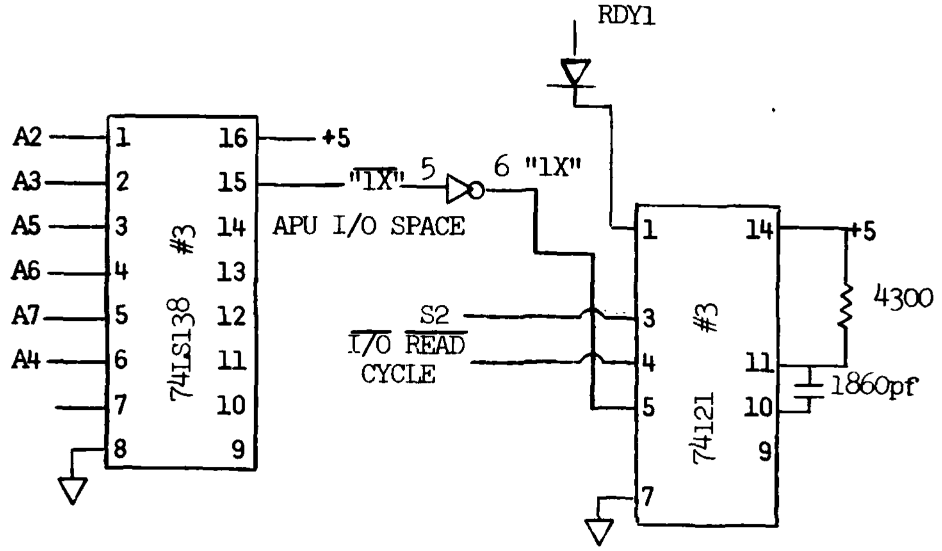


FIGURE 21. TIMING CIRCUITRY FOR APU DELAY

The diode at Pin 1 of the 74121 makes the totem pole output of the 74121 appear as an open collector device. This diode should be germanium to minimize potential drop across the diode. Whenever the 74121 is enabled by the 1x IO space being addressed, the delay is triggered if an IOR cycle is decoded or S2 goes to zero. Figure 22 shows a similar circuit for the hybrid subsystem.

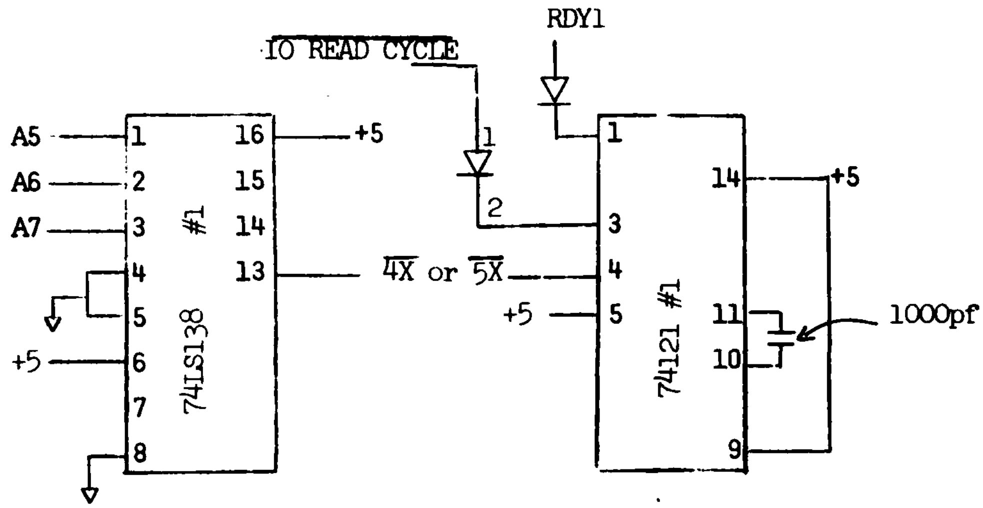


FIGURE 22. HYBRID READ DELAY CIRCUIT

In this circuit the status is presented early in T1 and addressing later. If an IO Read cycle is to take place pin 3 will be high enabling the 74121 #1 so that when the hybrid space is addressed pin 4 will go low and the 74121 will be triggered causing a delay to the processor. 74121 #2 is used in an identical manner to delay all I/O activity with the WD1791 and the 8257 in address space "CX" or "DX".

IV. THE CPU BOARD

The CPU board contains the 8086 CPU, its essential support chips, the ready circuit controller for slow memory and I/O, the DMA control circuit and the interrupt controller along with its supporting decoding circuitry. This board, like most others in the system, is very densely populated but easy to understand when considered in its component parts. Figure 23 shows an overview of the CPU Board.

The CPU and its Essential Support Chips

The CPU of the USAFA/8086 is connected in the maximum mode (6:10) and utilizes the Intel 8284 Clock Generator and the 8288 System Controller. The address latchs are 8282's and the data lines are buffered by 8286's. Some of the essential system control lines are buffered through an 81LS95. Figure 23 shows the CPU and its attendant supporting integrated circuits.

The CPU is run at a clock rate of 4 MHz (250 ns cycle). Although higher speed 8086's have been introduced since system design was initiated, and in fact this system has been run as fast as 5.25 MHz (191 ns), the 4MHz speed was chosen to avoid access and timing difficulties with memory and I/O support as well as to minimize noise. At the 250 ns cycle time a read cycle ($\overline{RD}$ valid) may be as short as 345 ns. At the 190 ns clock rate, the read cycle should be expected to last no longer than 225 ns.

The maximal mode of operation was initially chosen to allow for future expansion to multiprocessing environments and compatibility with projected Intel future components. The advantages of using this mode and, in fact, the capabilities of the 8288 system controller to provide adequate signals are certainly questioned by the research of this system.

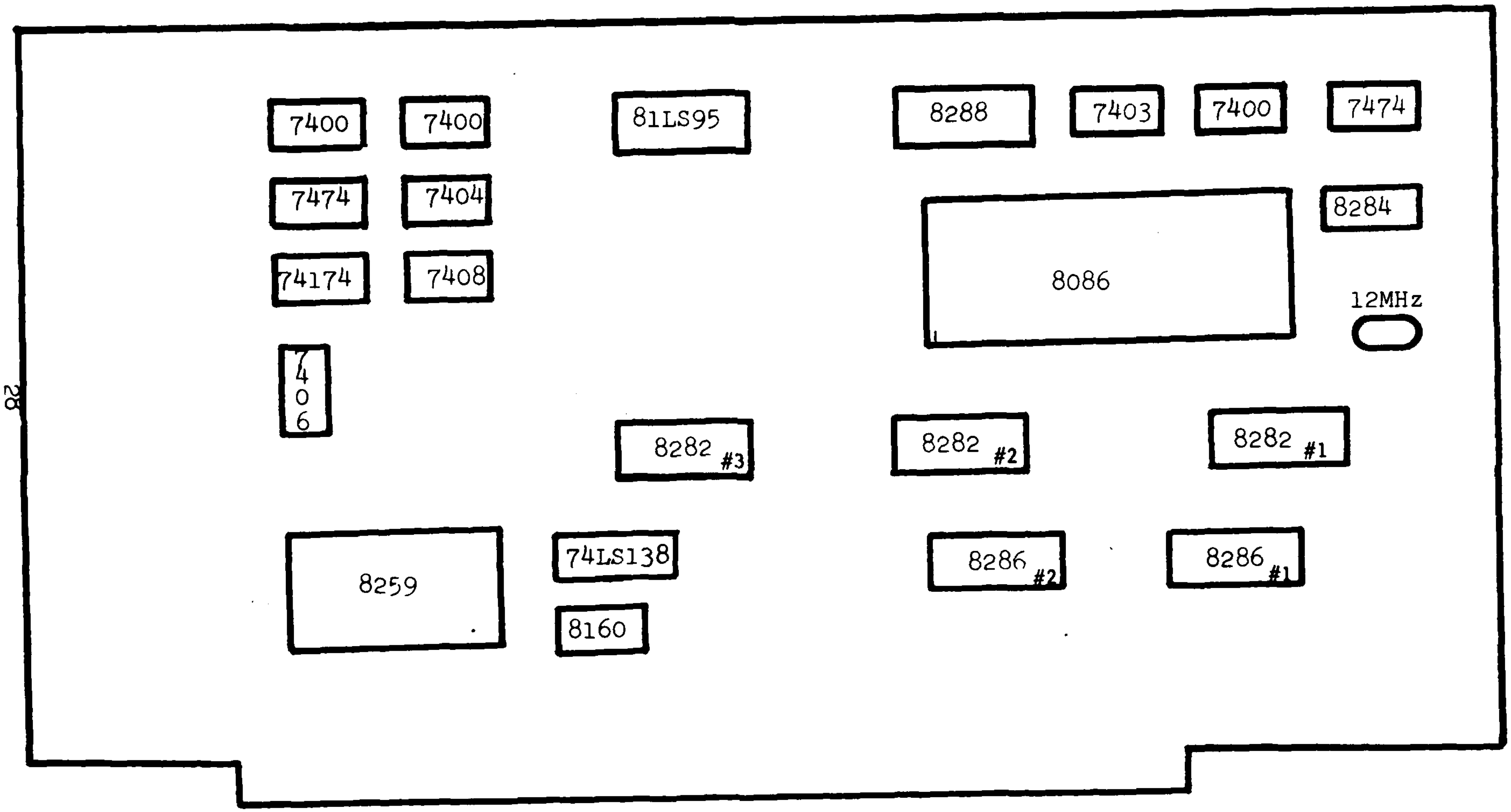


FIGURE 23. CPU CARD

For example, decoding done using the 8288 system controller output signals proved to be inadequate to support use of the system's RDY line necessitating the use of decoders operating directly on the CPU status lines which are the same lines used by the 8288 itself. The implementation of an on-board system DMA controller was necessitated by the awkward nature, critical timing, and synchronous actions of the $\overline{RQ}/\overline{GT}$ DMA control lines. No existing peripherals at the time of this system design would support such an operating environment.

Additionally, the system clock generator 8284 seems to have difficulty operating at the higher frequencies. No circuit provided by the manufacturer at the time of purchase proved to be satisfactory on system power on and reset. The series capacitor suggested by the manufacturer proved ineffectual and forced separate investigation (6:28).

The System CPU

The 8086 CPU shown in Figure 24 provides the nucleus about which the USAFA/8086 is built. To provide adequate discussion of this circuit would merely be a reiteration of the manufacturer's specification (6:3-21). The signals provided to and from the CPU are buffered to protect one of the more expensive single IC's in the system. The AD0 to AD15 lines are demultiplexed by the 8282's prior to the signals leaving the CPU board. Table 6 shows the source/destination of the CPU signals.

The System Clock Generator

The 8284 is connected as shown in Figure 25. The external frequency input is connected to the rear panel of the computer through coaxial cable. The frequency/crystal (F/$\overline{C}$) select switch is also routed to the rear panel along with power and ground to allow clock source selection. The external clock should be a TTL level signal. Experience shows the system will not

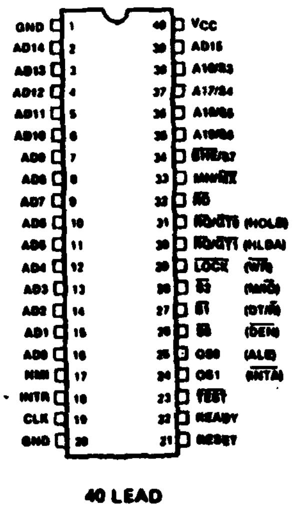


FIGURE 24. 8086 PIN OUT

TABLE 6. CPU SIGNAL DISTRIBUTION

PIN	NAME	I/O	SOURCE/DESTINATION
1	GND	I	Power Supply
2	AD14	I/O	8286#2 Pin #7 8282#2 Pin#7
3	AD13	I/O	8286#2 Pin #6 8282#2 Pin#6
4	AD12	I/O	8286#2 Pin #5 8282#2 Pin#5
5	AD11	I/O	8286#2 Pin #4 8282#2 Pin#4
6	AD10	I/O	8286#2 Pin #3 8282#2 Pin#3
7	AD9	I/O	8286#2 Pin #2 8282#2 Pin#2
8	AD8	I/O	8286#2 Pin #1 8282#2 Pin#1
9	AD7	I/O	8286#1 Pin #8 8282#1 Pin#8
10	AD6	I/O	8286#1 Pin #7 8282#1 Pin#7
11	AD5	I/O	8286#1 Pin #6 8282#1 Pin#6
12	AD4	I/O	8286#1 Pin #5 8282#1 Pin#5
13	AD3	I/O	8286#1 Pin #4 8282#1 Pin#4
14	AD2	I/O	8286#1 Pin #3 8282#1 Pin#3
15	AD1	I/O	8286#1 Pin #2 8282#1 Pin#2
16	AD0	I/O	8286#1 Pin #1 8282#1 Pin#1
17	NMI	I	81LS95 Pin #13
18	INTR	I	8259A Pin#17
19	CLK	I	8384 Pin#8
20	GND	I	Power Supply
21	RESET	I	8284 Pin#10
22	READY	I	8284 Pin#5
23	TEST	I	81LS95 Pin#11
24	QS1	0	81LS95 Pin#6 Bus Pin #20
25	QS0	0	81LS95 Pin#8 Bus Pin #21
26	S0	0	8288 Pin#19 81LS95 Pin#19
27	S1	0	8288 Pin#3 81LS95 Pin#2
28	S2	0	8288 Pin#16 81LS95 Pin#18
29	LOCK	0	81LS95 Pin#4
30	RQ/GT1	I/O	DMA Hold Controller CPU Board 7406 Pin#12
31	RQ/GT2	I/O	1K Pull-Up to +5
32	RD	0	N/C
33	MN/MX	I	Grounded to Achieve Maximal System
34	BHE	0	8282 Pin#5 To Bus Pin#74
35	A19	0	8282#3 Pin#4
36	A18	0	8282#3 Pin#3
37	A17	0	8282#3 Pin#2
38	A16	0	8282#3 Pin#1
39	AD15	I/O	8286#2 Pin#8 8282#2 Pin#8
40	+5	I	Power Supply

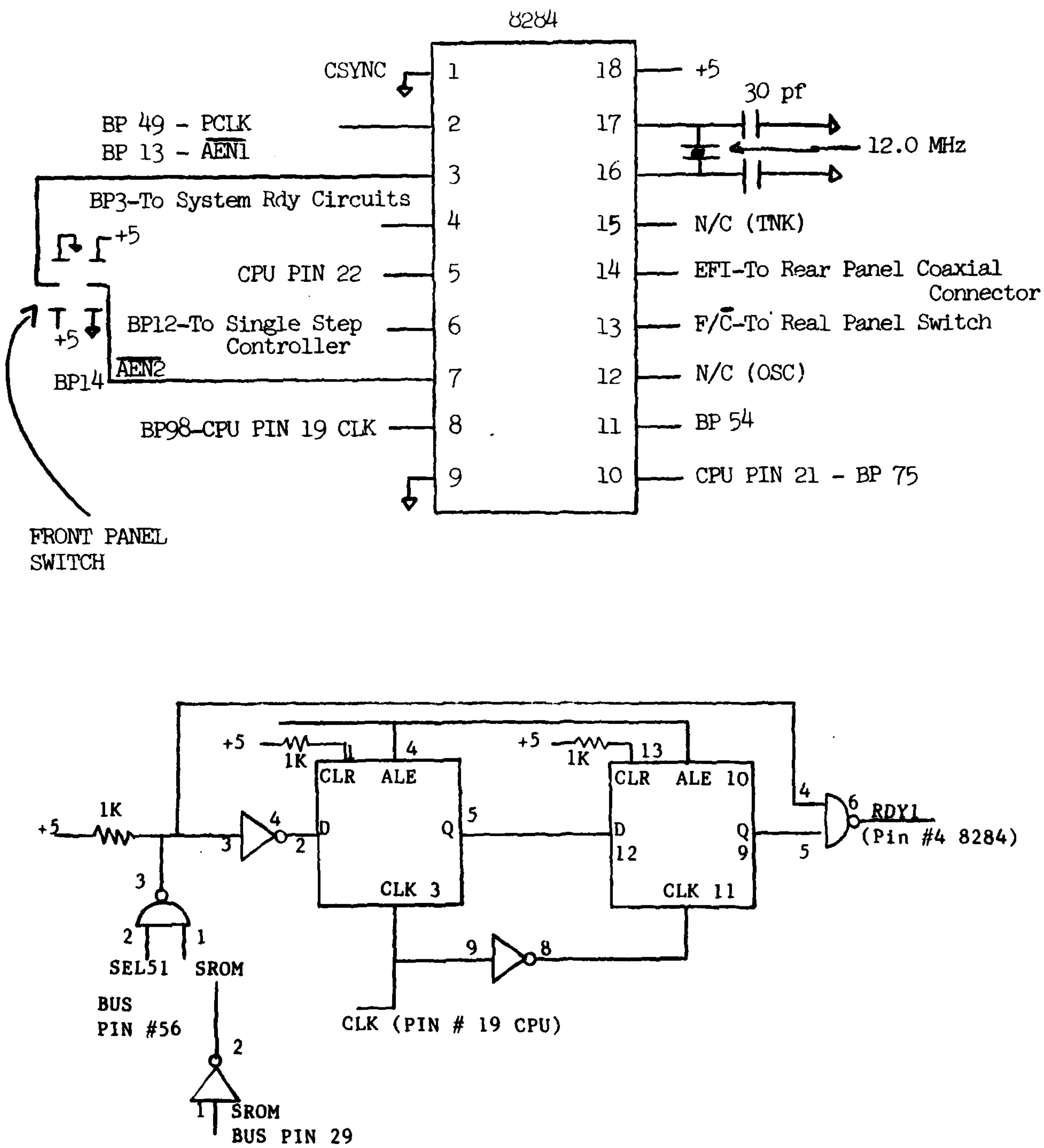


FIGURE 25. CLOCK GENERATOR/SYSTEM READY CONNECTIONS

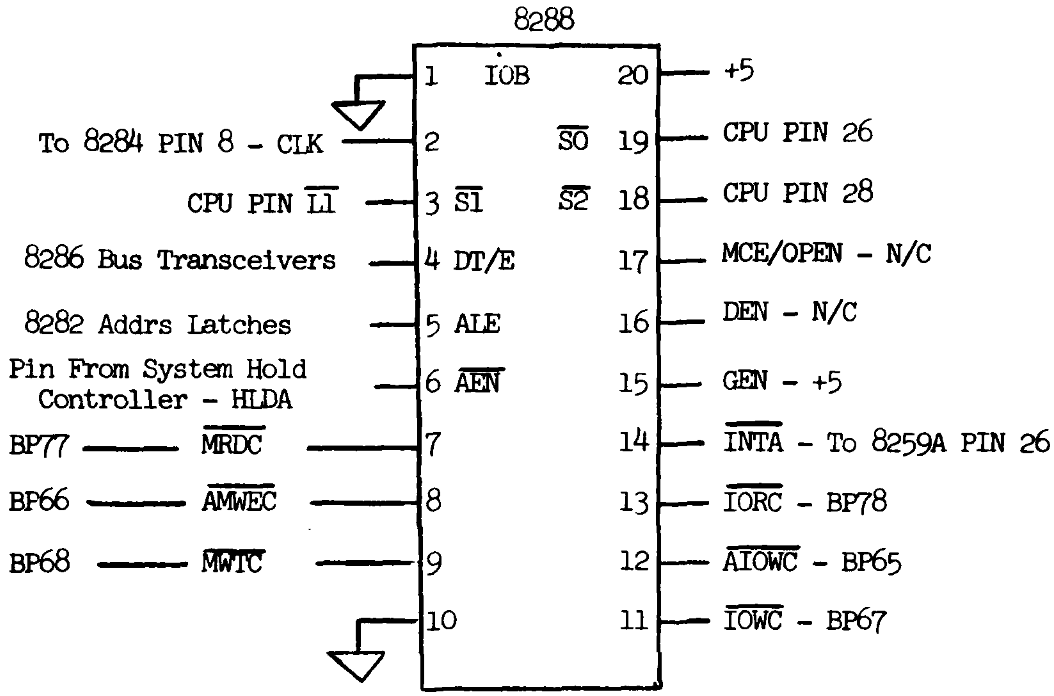


FIGURE 26. SYSTEM CONTROLLER

run properly on crystal when the external frequency input is powered, whether or not it is selected. It is conjectured this is due to mixing occurring internal to the 8284.

The System Controller

The 8288 is connected in the system bus mode (6:38) and serves to provide the system with the essential control signals required for operation based on CPU status lines S_2, S_1 and S_0. The $\overline{AEN}$ line is connected to the HLDA line generated by the system DMA controller described later in this chapter. Figure 26 shows the pin connection to the system controller.

The System RDY Controller

The 8086 system RDY line (Pin 22) is controlled through the 8284 system clock generator. The clock generator has two RDY line inputs called RDY1 and RDY2. These are gated through the 8284 by two enables called $\overline{AEN1}$ and $\overline{AEN2}$ respectively (5-25). Either or both of these systems may be activated simultaneously. In the USAFA/8086 these systems are used separately. The RDY1 line is the primary line which is used during normal system operations while running. The RDY2 line is used in conjunction with the system single step unit. The front panel contains a double pole single throw switch which is labeled RUN/SS and allows choice of mode of operation for the system.

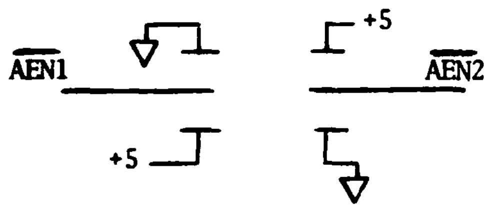


FIGURE 27. FRONT PANEL RUN/SS SWITCH

By using the switch as shown in Figure 27 only one of the RDY systems may be selected at a time. The circuit attached to the RDY2 line is discussed in Chapter II with the single step controller. The primary system attached to RDY1 (Figure 25) is the one originally suggested by the manufacturer when he supplied the MCS-86 kits used in the original design of the system. No explanation of circuit function was provided by Intel; however, analysis of the system timing leads to the timing diagram of Figure 29. This shows the circuit introduces one and only one wait state in every access to ROM (slow memory) and also the 8250 series I/O chips. We note that only address signals are used to drive this circuit and hence it is able to reach the CPU in adequate time to insert a wait state in the desired CPU cycle. Other circuits are also attached to the open collector RDY1 line and are described with the front panel board, the APU board, and the disk controller board.

DMA Control

To simplify the process of DMA while using the 8086 in its maximal mode a special controller is required. The primary purpose of the controller is to provide a two line handshake pair ($\overline{HLDR}/\overline{HLDA}$) (hold request and hold acknowledge) rather than utilize the one line pulsed response system preferred by the 8086 and employed to minimize the number of CPU pins required for this function. Figure 28 shows the pulsed handshake versus the two line handshake.

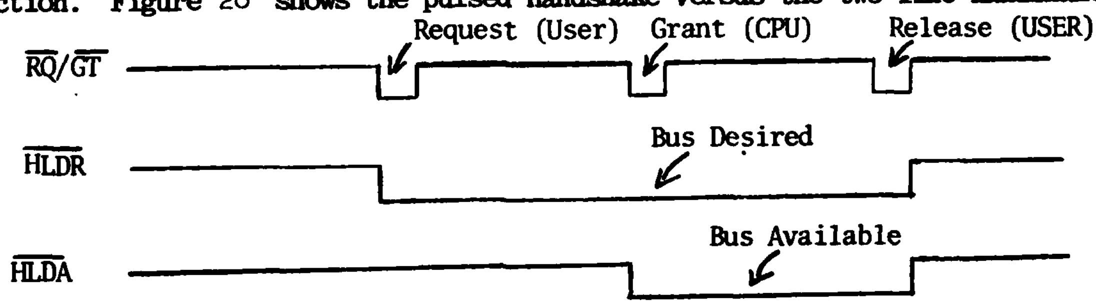


FIGURE 28. DMA SIGNALS

If the $\overline{RQ}/\overline{GT}$ logic is used each DMA device must have its own controller capable of providing and interpreting these signals. This controller is not simple

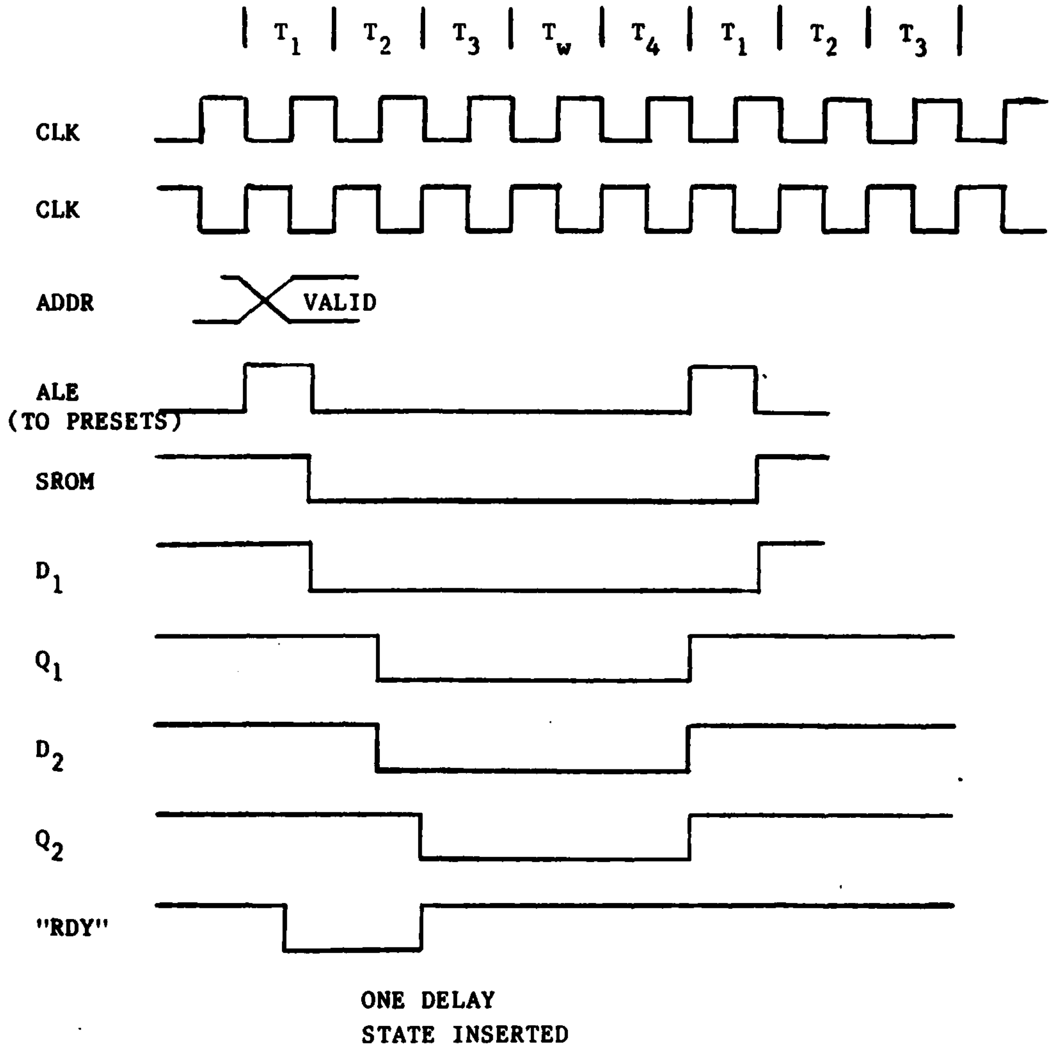


FIGURE 29
TIMING DIAGRAM - READY CIRCUIT

and consumes considerable board space. Thus it was decided to place a single controller available to all DMA devices on the CPU board. In constructing this controller it is necessary to realize that the pulses provided to the CPU must be exactly one clock pulse wide and synchronized the CPU clock whereas the CPU pulse ($\overline{GT}$) is not necessarily synchronous. Figure 30 shows a state diagram of the required controller. This controller could have been implemented in any of the many available conventional methods. For ease of trouble shooting and due to the small number of states, a one hot controller (one flip flop/state) was chosen.

Figure 31 shows the direct implementation of the state diagram using and/or logic in conjunction with D type flip flops. To minimize the number of types of gates required, this diagram was then converted to NAND/NAND logic with D flip flops as shown in Figure 32. Finally, Figure 33 shows the implementation actually used. The pin numbers and IC numbers on this drawing reflect the final configuration. A single D flip flop is used to "synchronize" the asynchronous HLDR signal issued by the requesting DMA devices. The overall system design prohibits the simultaneous request of the bus from several external sources.

System Interrupt Controller

The Intel 8259A, programmed to operate as a single master utilizing memory locations 00080_H thru $009F_H$ for vectors in the 8086 mode, serves as the system interrupt controller. This powerful LSI circuit is detailed in (6:42-59) the MCS86 Users Manual. Decoding for the 8259A is provided by the circuit in Figure 34. The interconnections to the 8259A are illustrated in Figure 35.

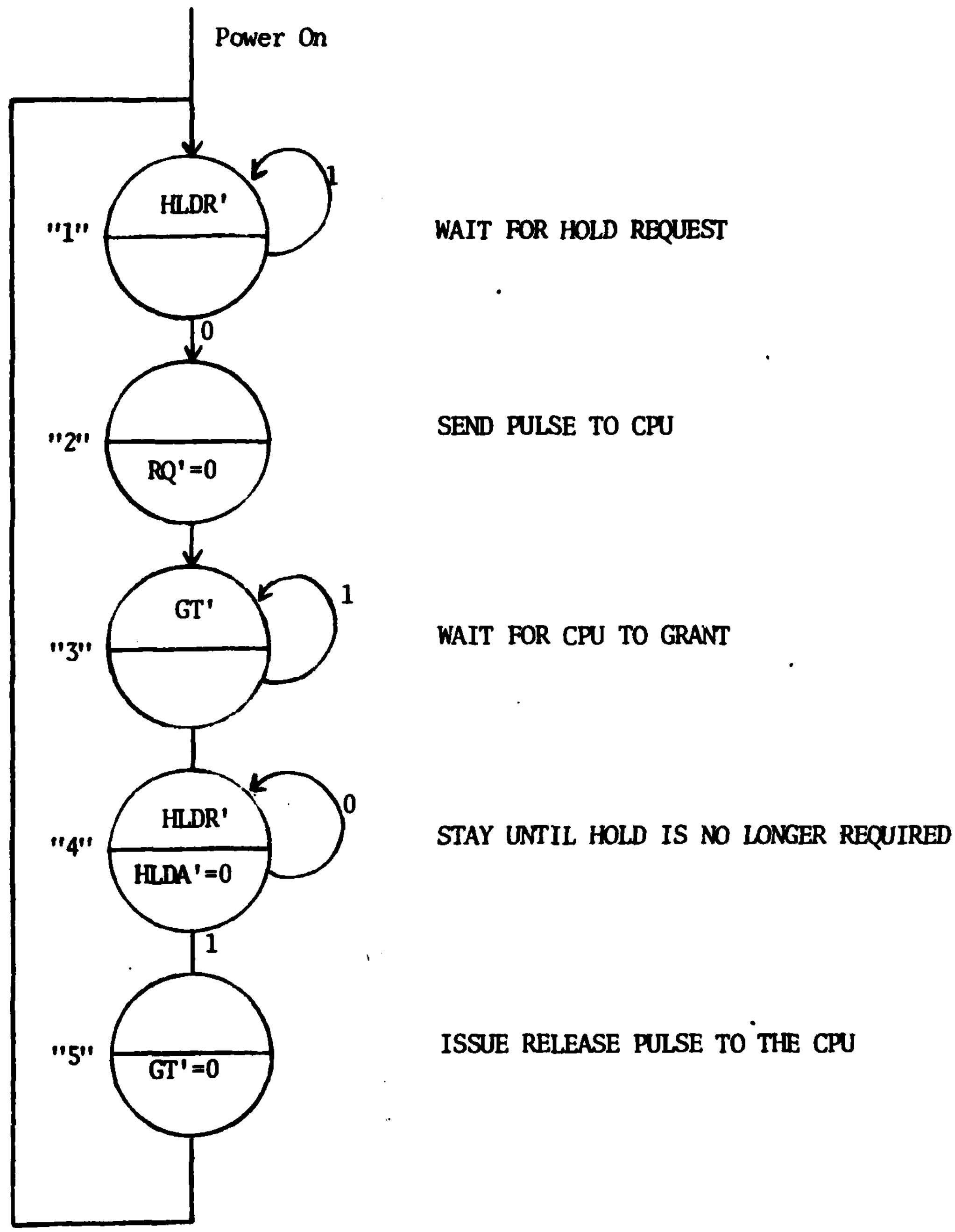


FIGURE 30
STATE DIAGRAM

ONE HOT CONTROLLER
STRAIGHT FORWARD DESIGN

1 - 74175	SFF's
1 - 7474	
2 - 7408	6 ANDS
1 - 7432	3 ORS
1 - 7406	6 NOT (OC)

(Same # as current except 1 7400)

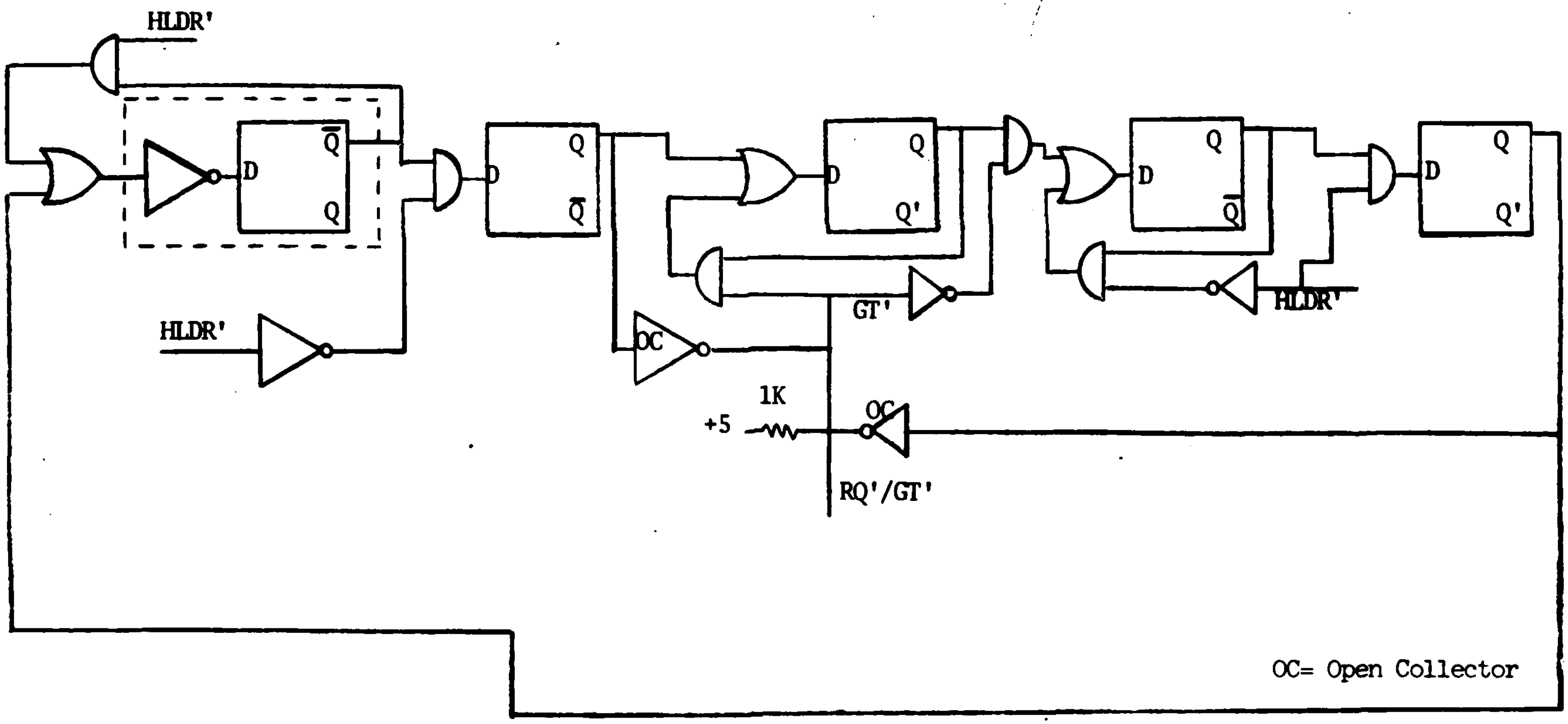
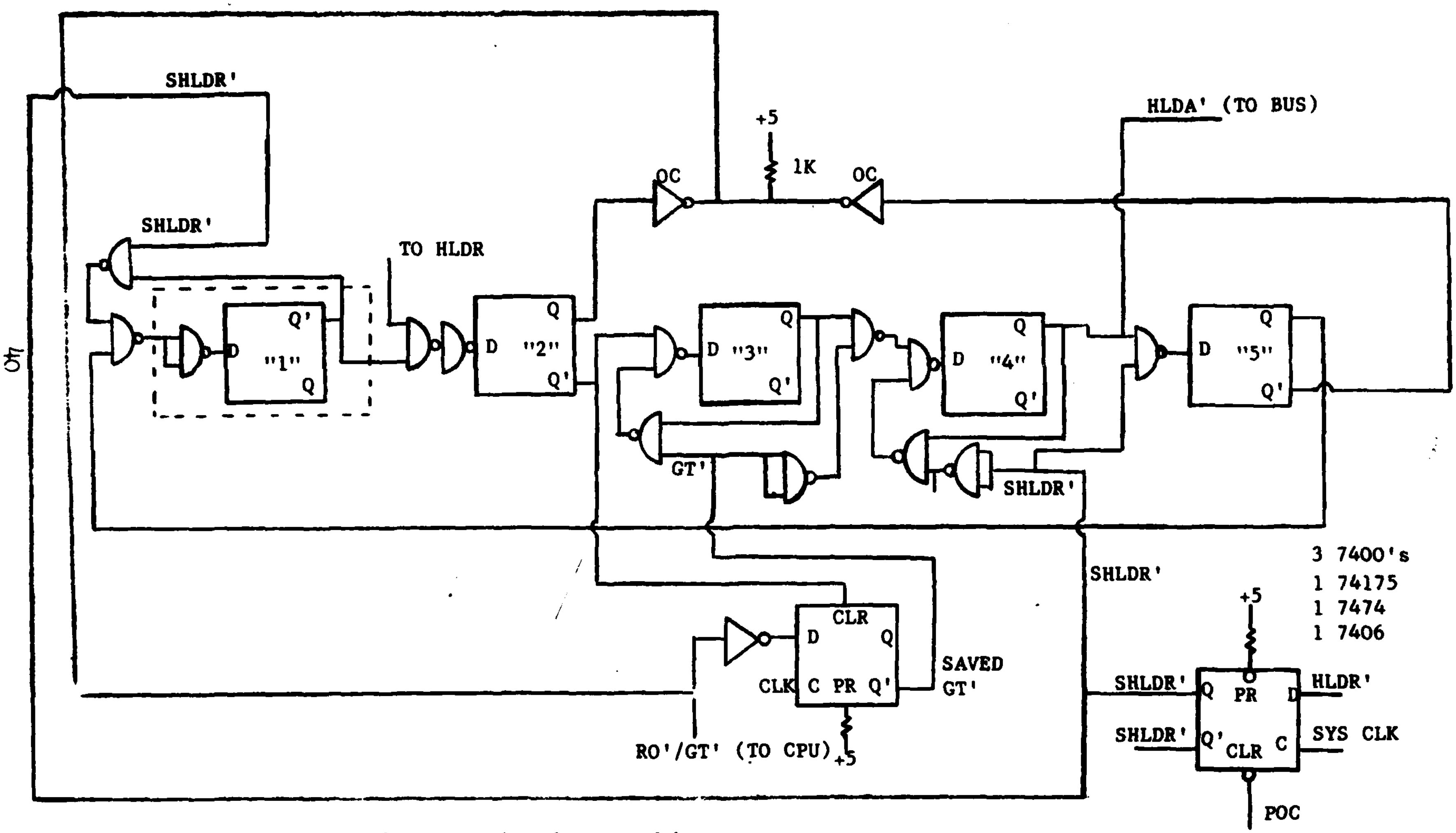


FIGURE 31. ONE HOT CONTROLLER

ONE HOT CONTROLLER
NAND IMPLEMENTATION



"Inverting" input on "2" cannot be eliminated because of Power On Clear Requirement. However, since "5" is a 7474, it can.

FIGURE 32. ONE HOT CONTROLLER

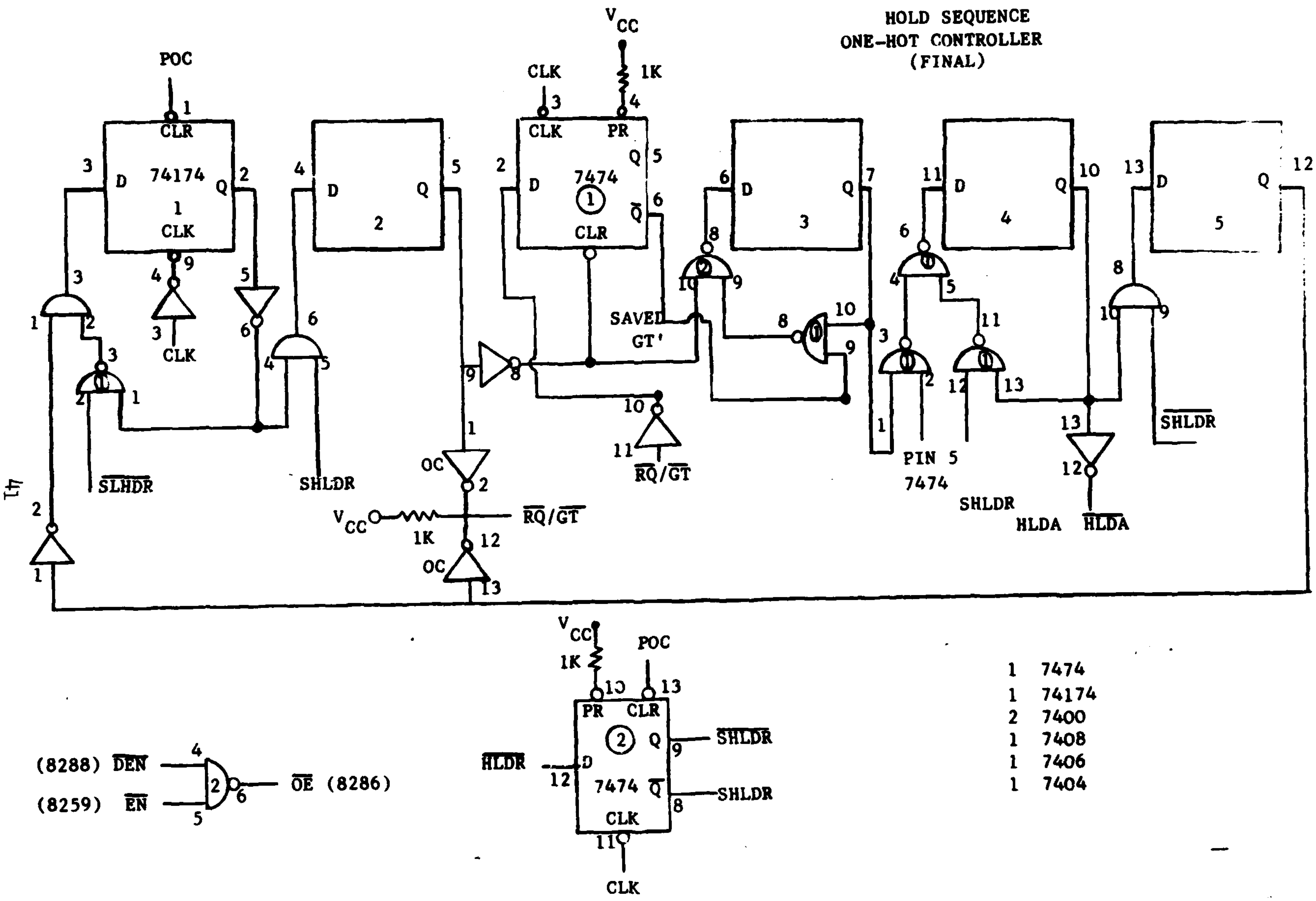


FIGURE 33. HOLD SEQUENCE

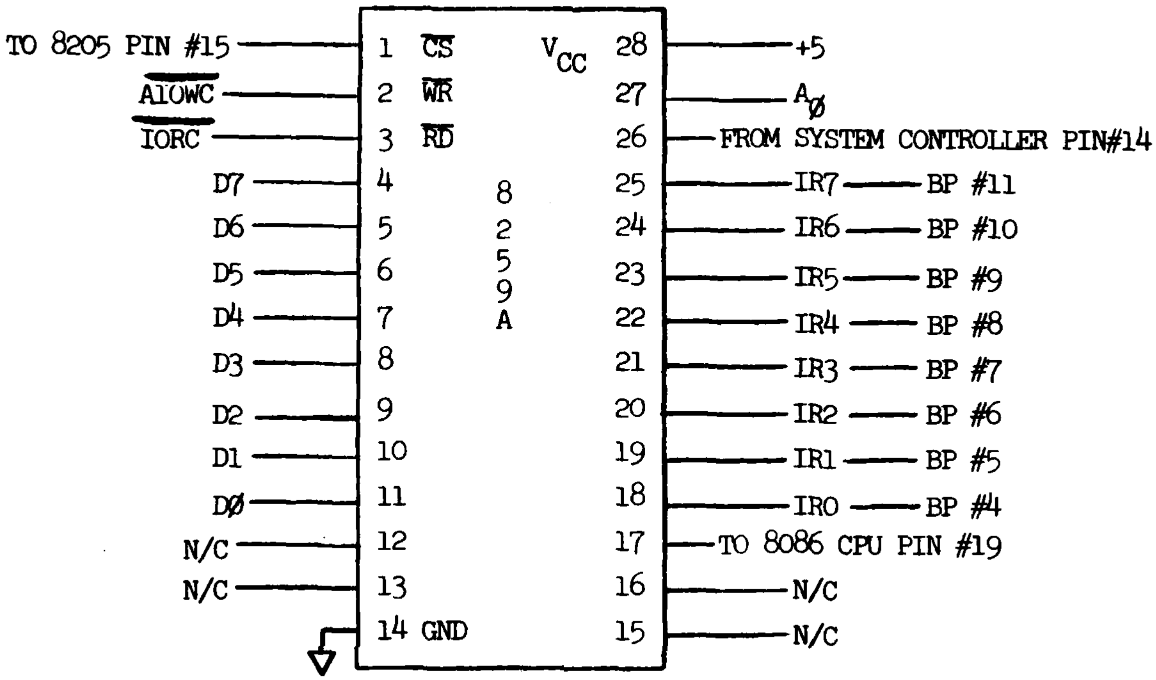


FIGURE 34. 8259A INTERRUPT CONTROLLER INTERCONNECTIONS

The interrupt controller interfaces its request lines directly onto the system bus (Pins #4 thru #11). The controller is programmed to be edge sensitive triggered and normally the interrupt request lines will be pulled low unless connected into the system by an octal switch pak located on the front panel board (See Chapter II). If a particular interrupt line is used in the system, the appropriate switch on the pak should be opened and control relinquished to the interrupt requesting device.

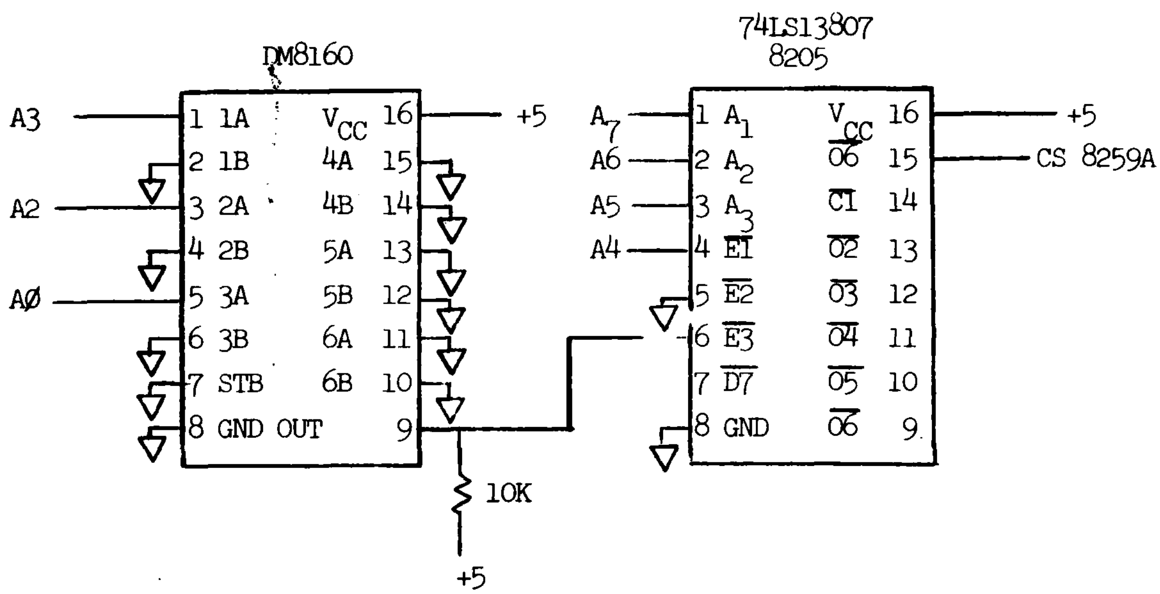


FIGURE 35. DECODING FOR 8259A INTERRUPT CONTROLLER
(DEVICE 00 AND 02)

V. EPROM/RAM MEMORY

The memory boards of the USAFA/8086 were the first boards completed for the system. The universal design of the board allows it to use those memories in the Intel 2716 family as well as those RAMs designed for compatibility. The board has several features in addition to its universal nature which include a write protect capability as well as a shadow masking capability. Neither of these features were actively used in the AFFDL version of the USAFA/8086. However, they are described in this chapter for completeness. The board is completely buffered to protect the expansive memories from the potential electrical atrocities of a bus oriented system. The board is shown in its ROM configuration (32K) in Figure 36 while Figure 37 shows the 16K RAM configuration.

Board Selection

The circuitry of Figure 38 is used for board and chip selection. The DM8160 is a high speed hex comparator. Since it is not a TTL compatible integrated circuit its active high output must be pulled up by a 10K resistor. When the board is configured to contain 1Kx8 memory circuits, the 8160 verifies that the uppermost six address lines (A14-A19) match the values indicated by setting switches on the octal dip switch pak (Figure 39). If all six lines match the desired value then the 74LS138 is enabled and the chip to be selected is determined by address lines A13-A11. If 2Kx8 memories are used to create a 32K byte memory board, the 8160 only decodes the uppermost five address lines while the 74LS138 decodes A14-A12. A11 is applied directly to all memory IC's.

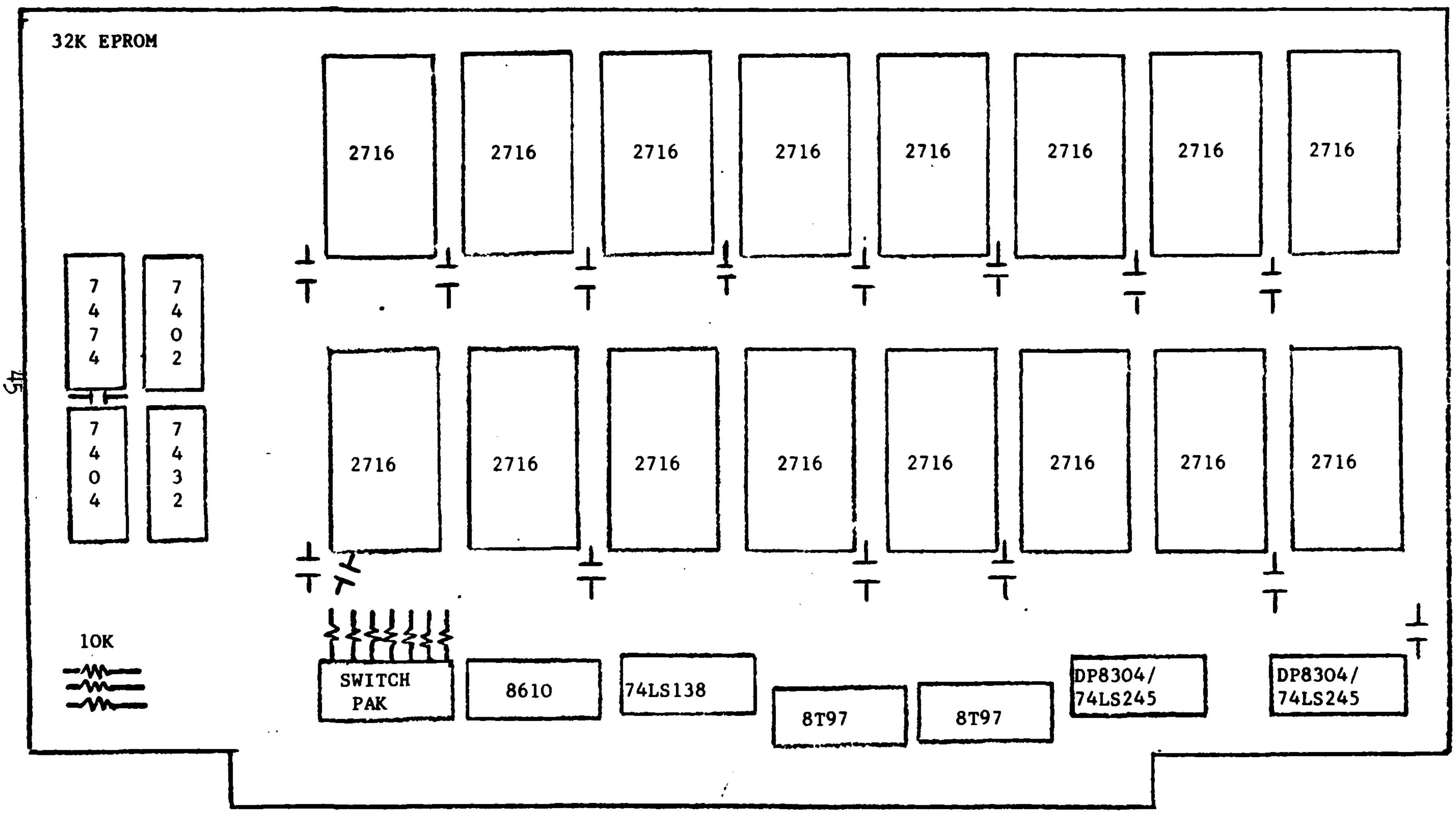


FIGURE 36. MEMORY BOARD PROM CONFIGURATION

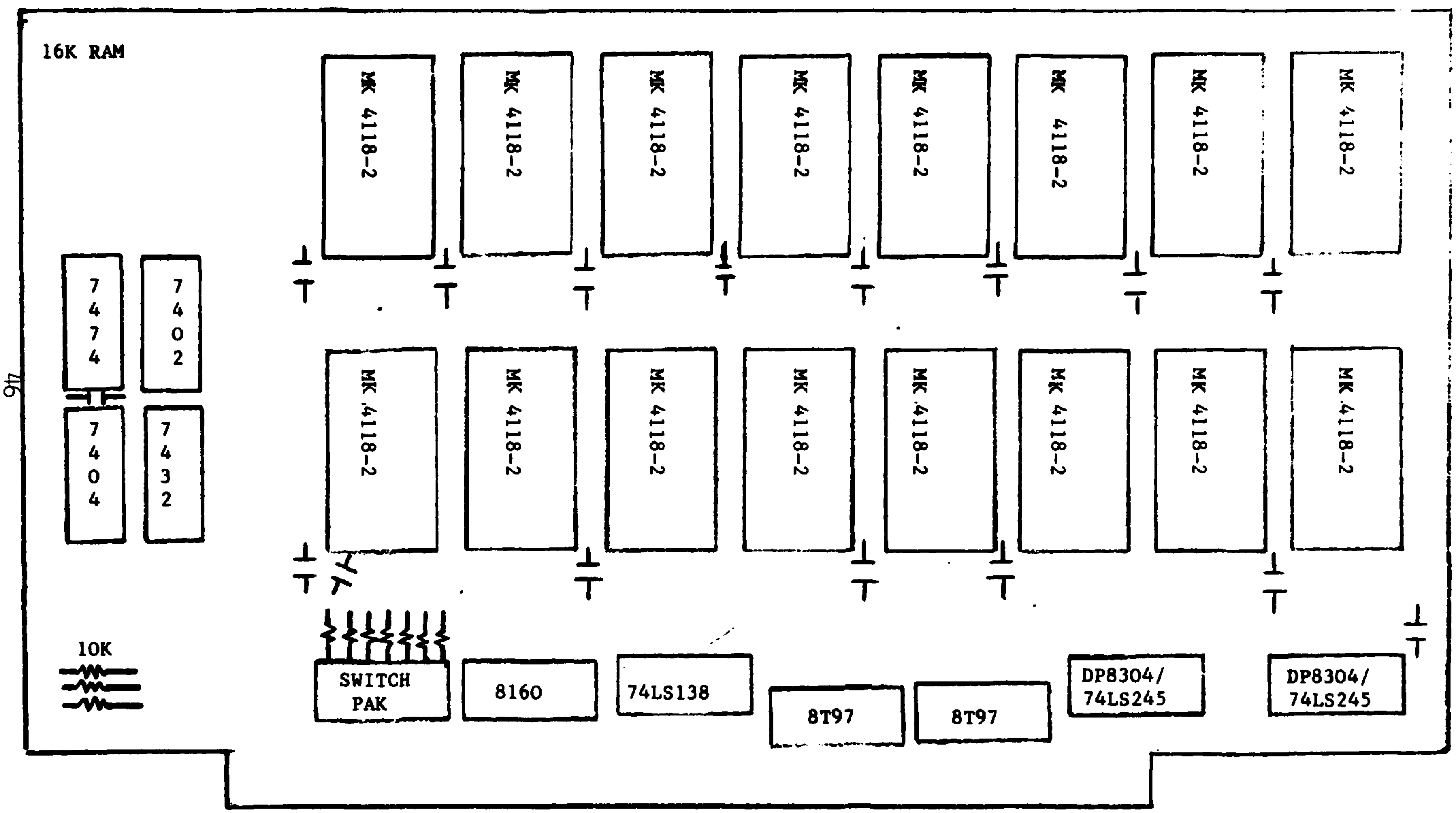


FIGURE 37. MEMORY BOARD RAM CONFIGURATION

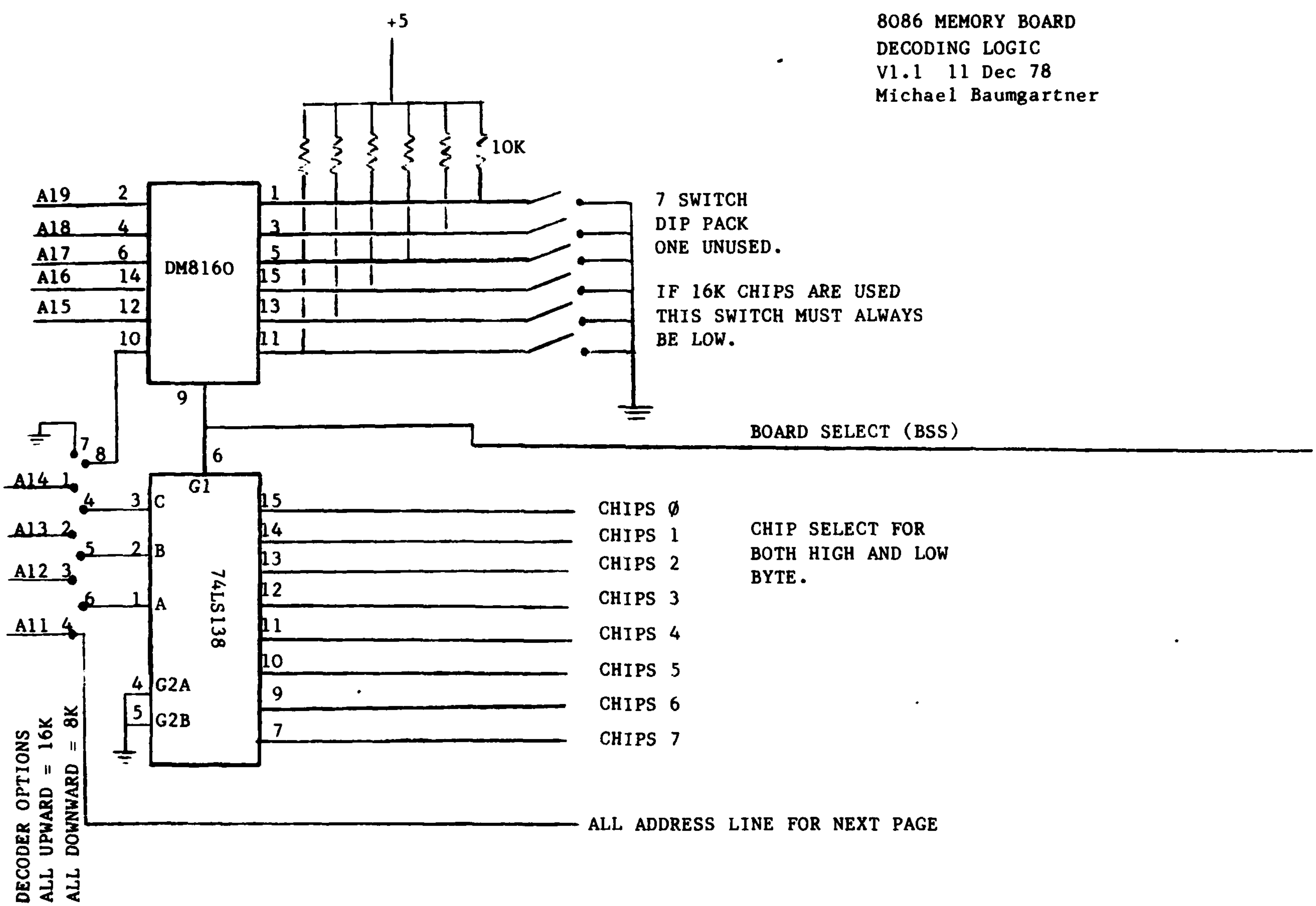


FIGURE 38. 8086 MEMORY BOARD

TO SELECT A CARD ADDRESS, DECIDE WHICH OF THE HIGH ADDRESS BITS ARE ONE'S AND ZERO'S AND SELECT THE SWITCH POSITIONS ACCORDINGLY.

'ON' = Ø
'OFF'= 1

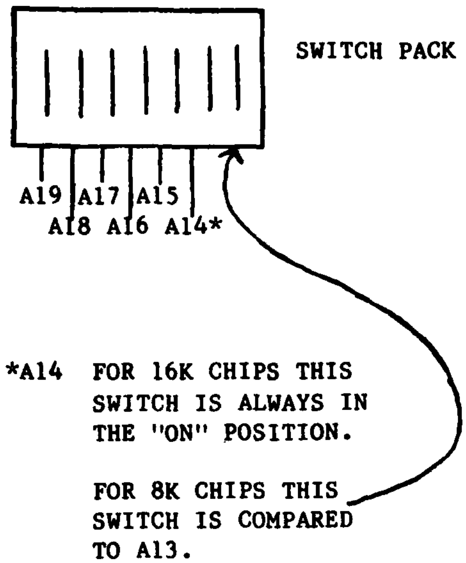


FIGURE 39. ADDRESS SELECTION

The Memory Enable

The memory chosen in addition to being selected must also have its output buffers enabled if the memory is to be read. In constructing the enabling logic three things are required: (1) A board select, BSS; (2) A memory read command, $\overline{MRDC}$; and (3) A special signal which indicates whether the board is RAM, ROM or a 50/50 combination of the two types of memory. This special signal allows for shadowing based on the bus signal called INH1. Shadowing is the process of enabling a ROM board located at the same physical address as a RAM board. This type of function is often useful in systems with a more limited address space (64K) than the 8086 (1M). If $\overline{INH1}$ = 0 and the board is wired by jumper as a RAM board, the board is disabled or shadowed while the corresponding ROM board will be enabled. A mixed memory board is independent of the $\overline{INH1}$ signal. Figure 40 shows the circuitry used to implement this logic.

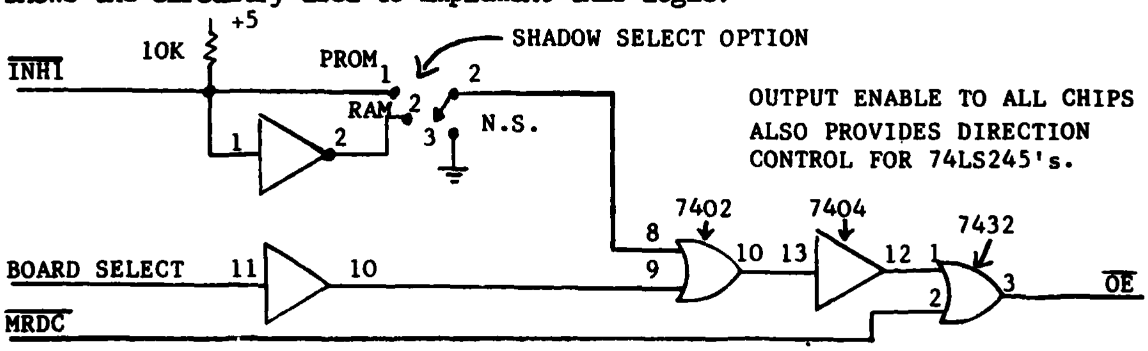


FIGURE 40. MEMORY ENABLE

Memory Protect (Write Inhibit) Circuitry

On those boards which are configured as RAM boards, in accordance with the byte oriented nature of the 8086, either the high (odd address) byte or the low (even address) or both may be written by a single instruction depending on the value of AØ and $\overline{BHE}$. Table 7 shows this relation.

TABLE 7 . MEMORY ACTIVITY

	AØ	$\overline{BHE}$
LOW BITE ONLY	0	1
HIGH BYTE ONLY	1	0
BOTH BYTES	0	0

Optionally the RAM board can be protected from any write in one of two ways. If the bus signal called $\overline{PROT}$ is pulled low all memory writes are inhibited. No stack operations are possible in this configuration. The boards may also be protected on a selective basis by setting a bit on the data bus and jumped on the board to 1 while strobing the $\overline{PS}$ line. If this memory write is not inhibited by either of these two methods, then the $\overline{AMWC}$ (Advanced Memory Write Command) is combined with AØ and $\overline{BHE}$ to generate the high and low byte write signals. The required circuitry to implement these functions is shown in Figure 41 .

Address Line Buffering

Both the address and data lines entering the memory card are buffered. Loading is not the primary consideration but rather component protection since each memory board contains as much as $800 in memory chips. Two 8T97's (7) are used for address buffering. They are always enabled. The circuit is shown in Figure 42 and their position on the memory board is indicated in Figure 45.

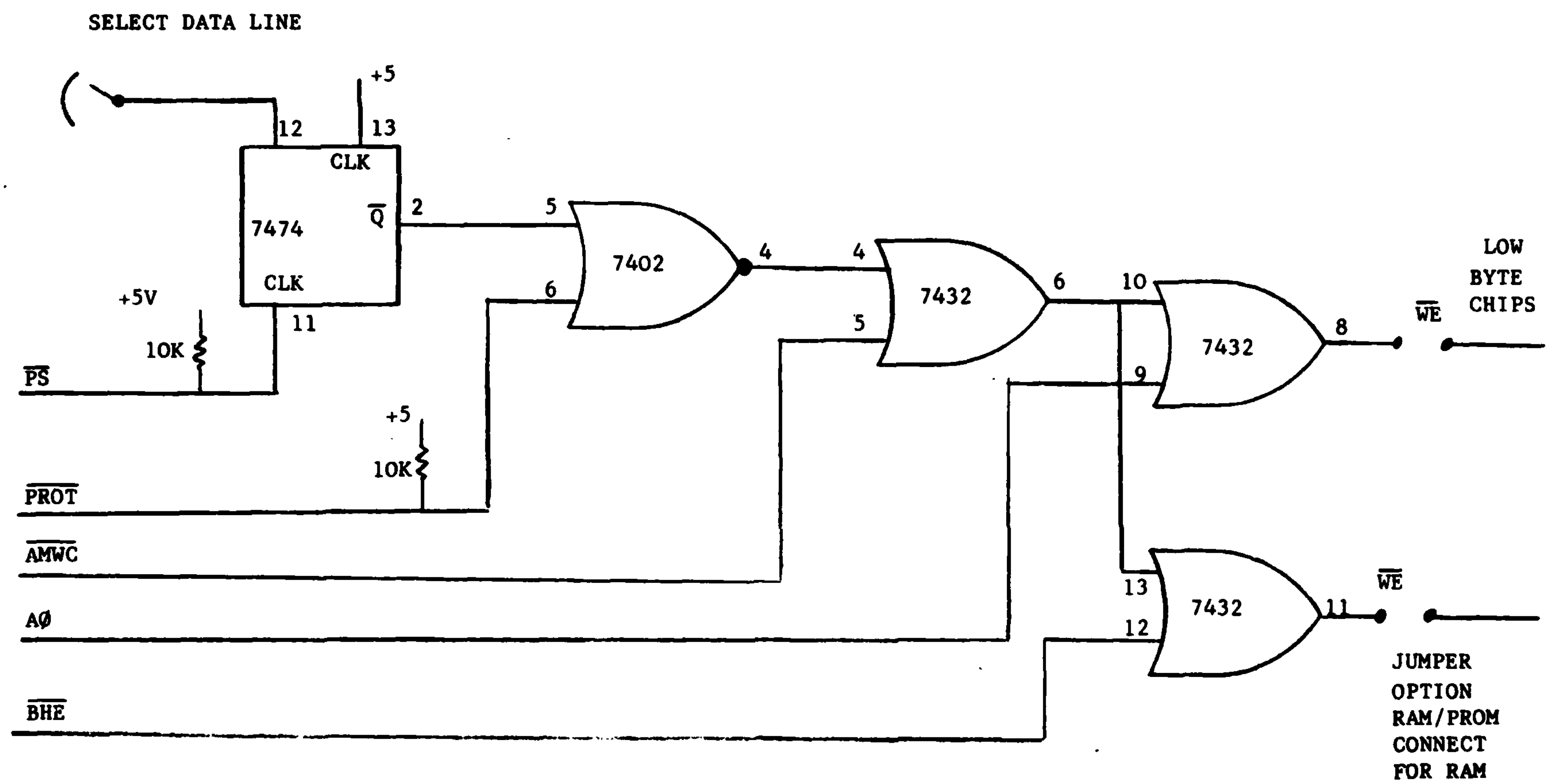


FIGURE 41. MEMORY PROTECT CIRCUITS

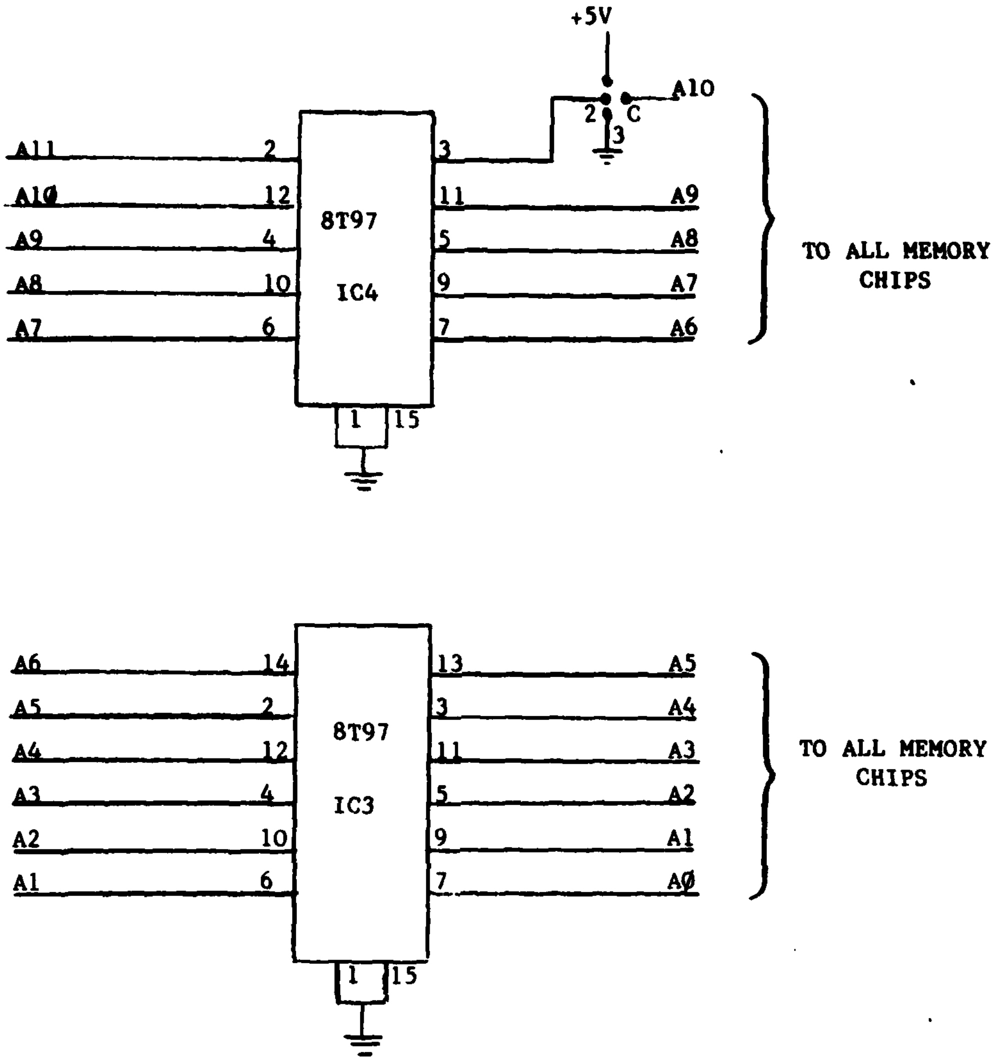


FIGURE 42. ADDRESS LINE BUFFERING

Data Line Buffering

Either of two IC's is used for data line buffering depending on the version of the board used. The original and more desirable design used 74LS245's (8) which remain difficult to obtain. The alternate design uses the DP8304 which is much more readily available. Figure 43 shows the 74LS245 implementation while Figure 44 shows the DP8304 (9) implementation.

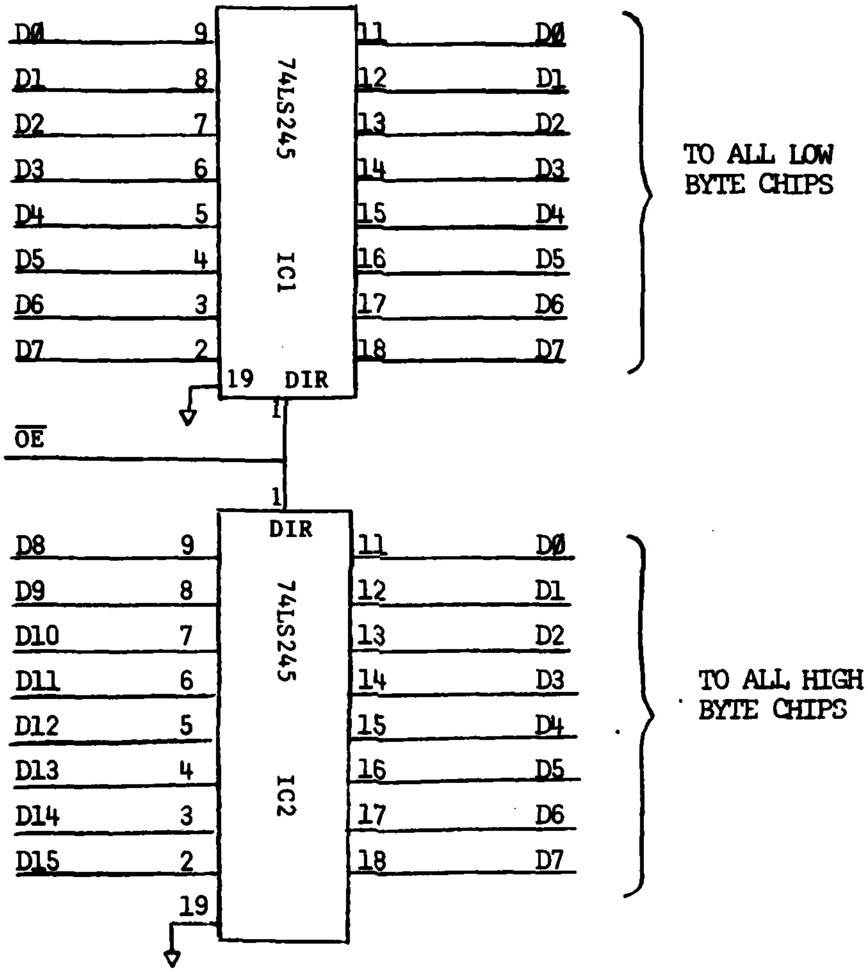


FIGURE 43. 74LS245 MEMORY DATA BUFFERING

These buffers are always enabled and facing into the memory board unless directed by the CPU to provide data on a memory read.

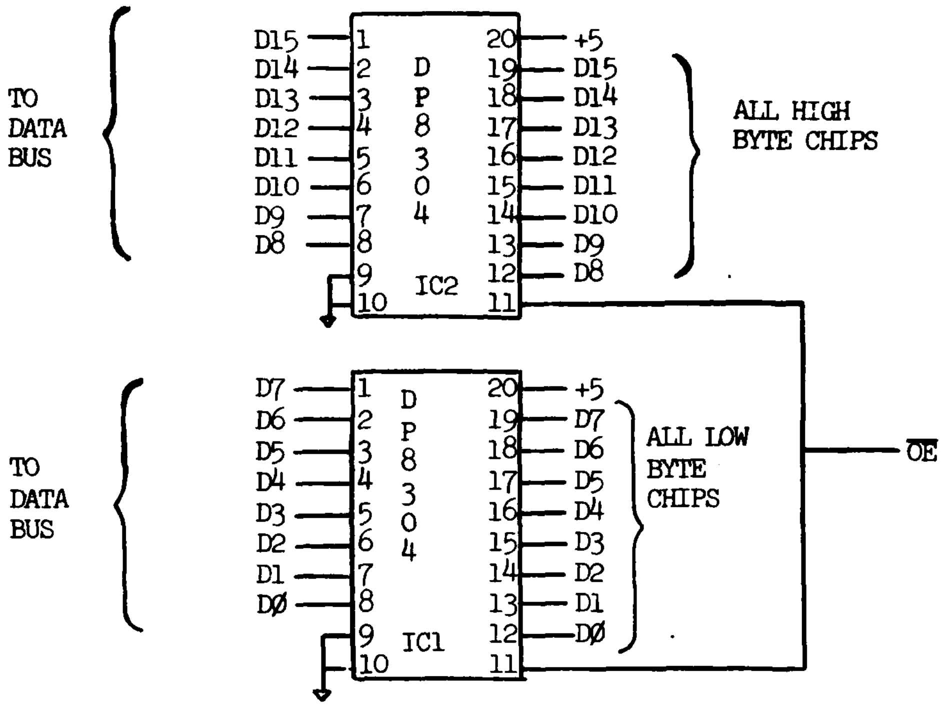


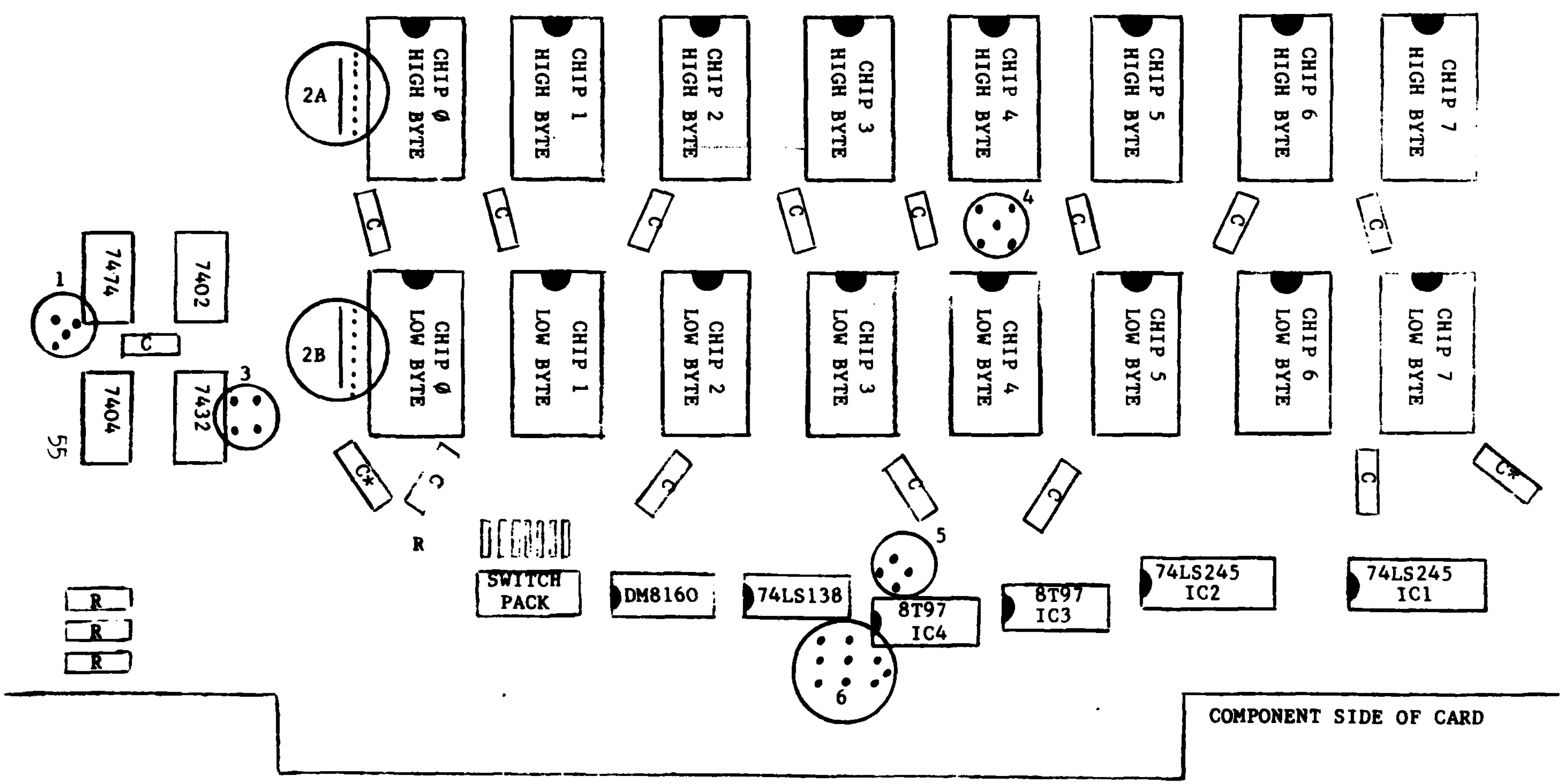
FIGURE 44. DP8304 MEMORY DATA BUFFERING

Memory IC's

The following memory chips are potentially usable on the memory board described in this chapter:

RAM		ROM	
1Kx8	MK4118	1Kx8	Intel 2758
2Kx8	AMIS5028	2Kx8	Mostek 2716
			Intel 2716
			TI 2516

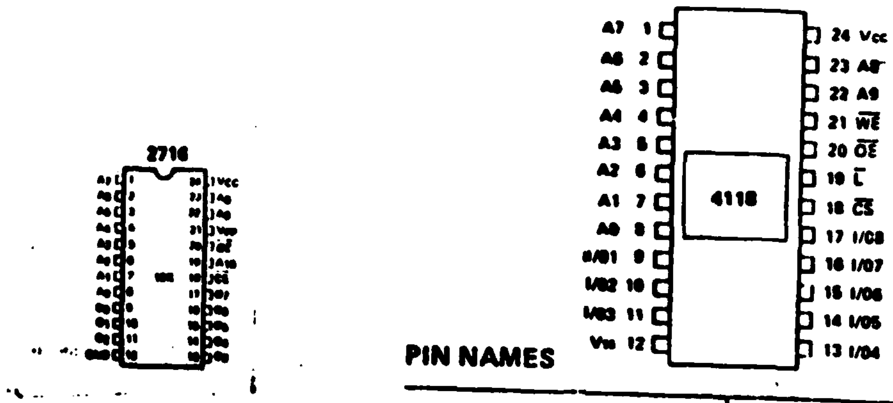
The pinouts for the Intel 2716 and the MK4118 which are currently used in the USAFA/8086 are shown in Figure 46.



ALL R's = 10K
ALL C's EXCEPT C* = .C1-.1μf
C* = 25μf TONTULUM

ALL STRAP OPTION AREAS ARE CIRCLED

FIGURE 45. MEMORY BOARD LAYOUT



PIN NAMES

A0 - A9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	$\overline{OE}$	Output Enable
Vss	Ground	$\overline{L}$	Latch
Vcc	Power (+5V)	I/O_1 - I/O_8	Data In/ Data Out Port

FIGURE 46. MEMORY CIRCUIT PINOUTS

These circuits are thoroughly described by their manufacturers (10:4-44) and (11).

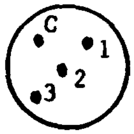
User Selectable Options

Figure 45 shows the user selectable option areas of the memory board. Table 8 expands each of these areas and shows the possible configurations.

TABLE 8 USER SELECTABLE MEMORY OPTIONS

<u>OPTION AREA 1</u>

BOARD SHADOW SELECT

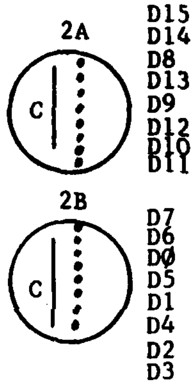


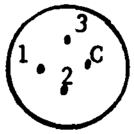
C=1 PROM
C=2 RAM
C=3 NON-SHADOWED

<u>OPTION AREA 2</u>

DATA BIT FOR WRITE-PROTECT STATUS

SELECT ONE OF THE 16 DATA LINES. IF WRITE-PROTECT IS NOT DESIRED CONNECT C TO GROUND.





<u>OPTION AREA 5</u>

COMBINE THIS OPTION AND OPTION 6 FOR SELECTION OF 8K CHIPS OR 16K CHIPS.

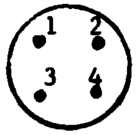
THIS OPTION DECIDES WHAT IS APPLIED TO PIN 19 OF THE MEMORY CHIPS.

FOR 16K CHIPS C=2. i.e., CONNECT A1Ø
FOR 8K PROM (2758) C=3
FOR 8K RAM C=1. (CHECK FOR PARTICULAR
RAM USED). MK4118

ALL OPTIONS ARE SHOWN FROM THE COMPONENT SIDE OF THE BOARD.

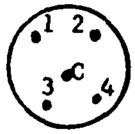
<u>OPTION AREA 3</u>

WE OPTION



IF RAM BOARD THEN CONNECT
1 = 2
3 = 4
IF COMBO OF RAM AND PROM THEN CONNECT
1 = 2
3 = 4
IF PROM, DO NOT CONNECT

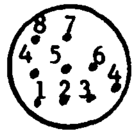
<u>OPTION AREA 4</u>



SELECT PROM, RAM OR COMBO MUST BE COORDINATED WITH OPTION AREA 3.

IF RAM ONLY CONNECT 1=2, 3=4, AND OPTION 3 (1=2, 3=4).
IF PROM ONLY CONNECT C=1=2=3=4 AND OPTION 3 (NOT CONNECTED)
IF RAM AND PROM C=2=4 AND OPTION 3 (1=2, 3=4)
IF RAM AND PROM THEN CHIPØ-CHIP3 ARE RAM AND CHIP4-CHIP7 ARE PROM

<u>OPTION AREA 6</u>



SELECT 8K CHIPS OR 16K CHIPS

FOR 16K CHIPS
1=4
2=5
3=6
7=8
4 NOT CONNECTED

FOR 8K CHIPS
4=6
3=5
2=4
1=8
7 NOT CONNECTED

VI. THE PARALLEL INPUT BOARD

This board was designed to provide general purpose parallel input ports to the computer system. Eight identical sixteen bit ports reside on the card. Each port may be addressed as a single sixteen bit port or as a pair of eight bit ports.

DECODING

Decoding is provided for the board by first determining if the board is selected and if so then which port is selected. Figure 47 shows the decoding method. Actual pin numbers used are designated.

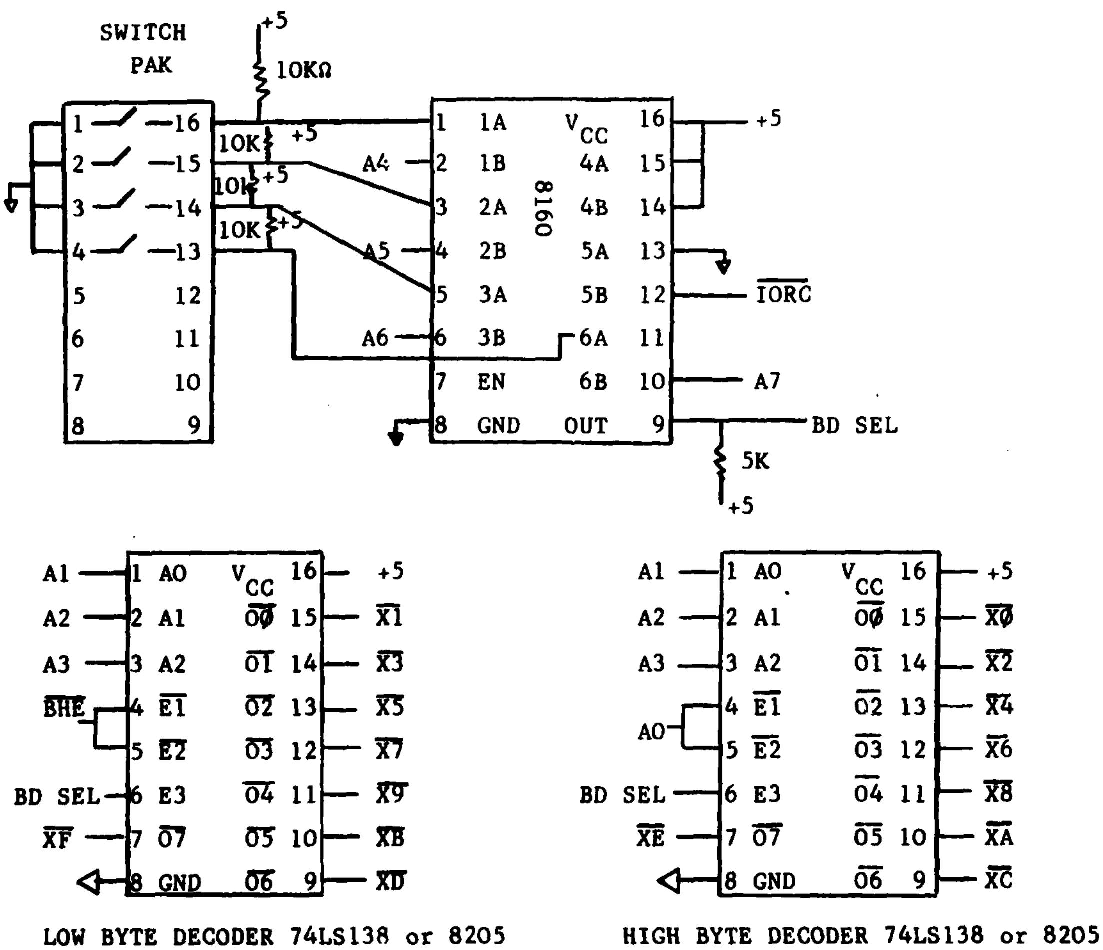
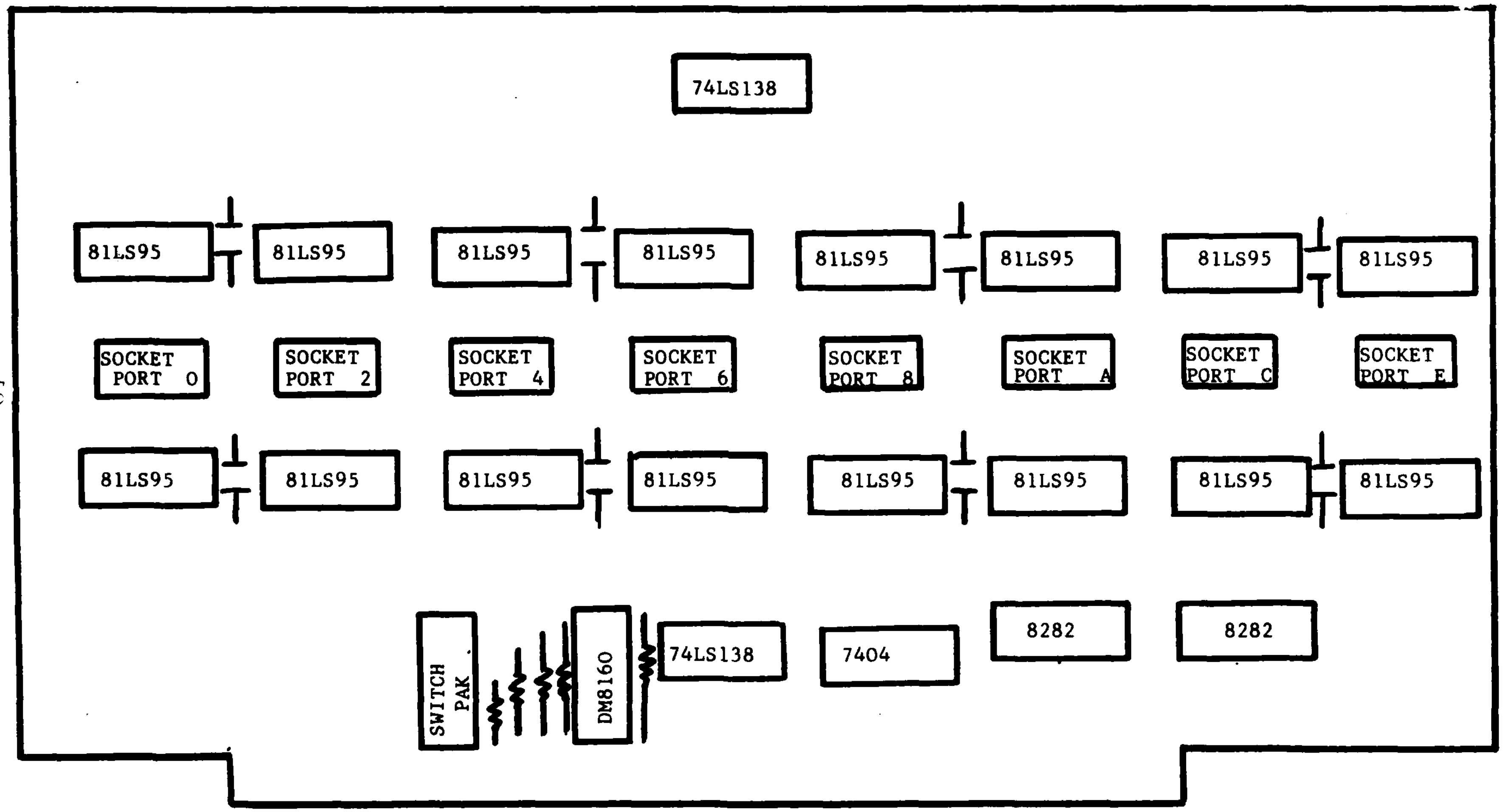


FIGURE 47. PARALLEL INPUT PORT DECODING



SYSTEM PARALLEL INPUT BOARD
FIGURE 48

BUFFERING

The outputs of the byte decoders go directly to the enable of the desired port. The data lines coming from the input board are buffered by use of 8282's (6:22). Figure 49 shows the pinout for these buffers.

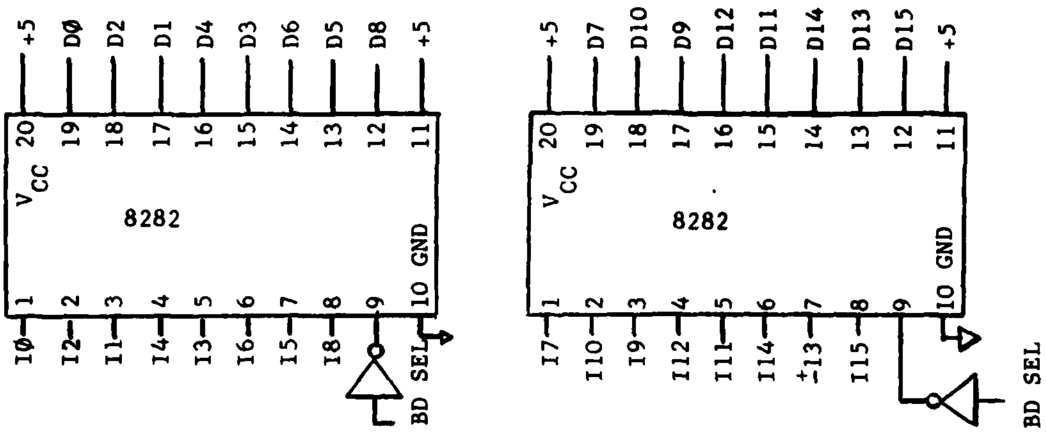


FIGURE 49. PARALLEL INPUT BOARD DATA BUFFERING

They are connected as tristate buffers since pin 11 is held high and they are enabled by the board being selected as described in Figure 47.

THE PORTS

Figure 50 shows an actual input port's connections.

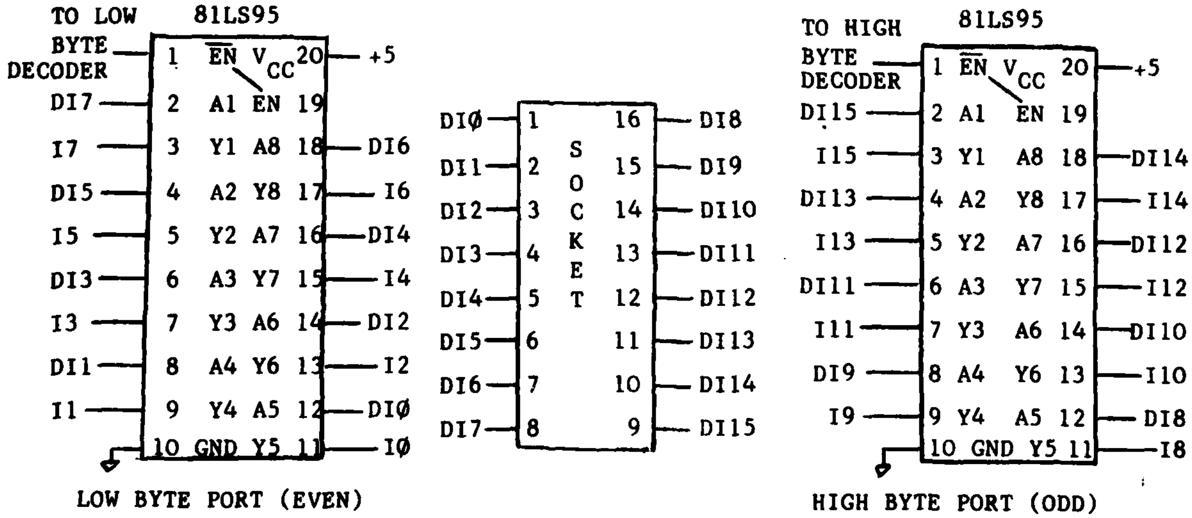


FIGURE 50. INPUT PORT CONNECTIONS

Since pins 1 and 19 of the input ports are connected either 81LS95 (12) or 81LS97 IC's are suitable for the application. Analysis of the 81LS95 or 81LS97's specifications leads to the conclusion that each input line from an external device is sourced a maximum of 20μa on a high input (>2.0 volts) and sinks a maximum of .36ma on a low input (<.8 volts). This is much less than 1 TTL load in either case.

VII. THE PARALLEL OUTPUT BOARD

The parallel output board, having been designed by the same individuals who designed the parallel input board, is extremely similar in physical appearance although different components are used for the ports themselves. The board contains eight sixteen bit ports which may also be addressed as eight bit ports.

DECODING

Decoding is determined first for the board and then for the particular port as shown in Figure 51. Actual pin numbers used are designated.

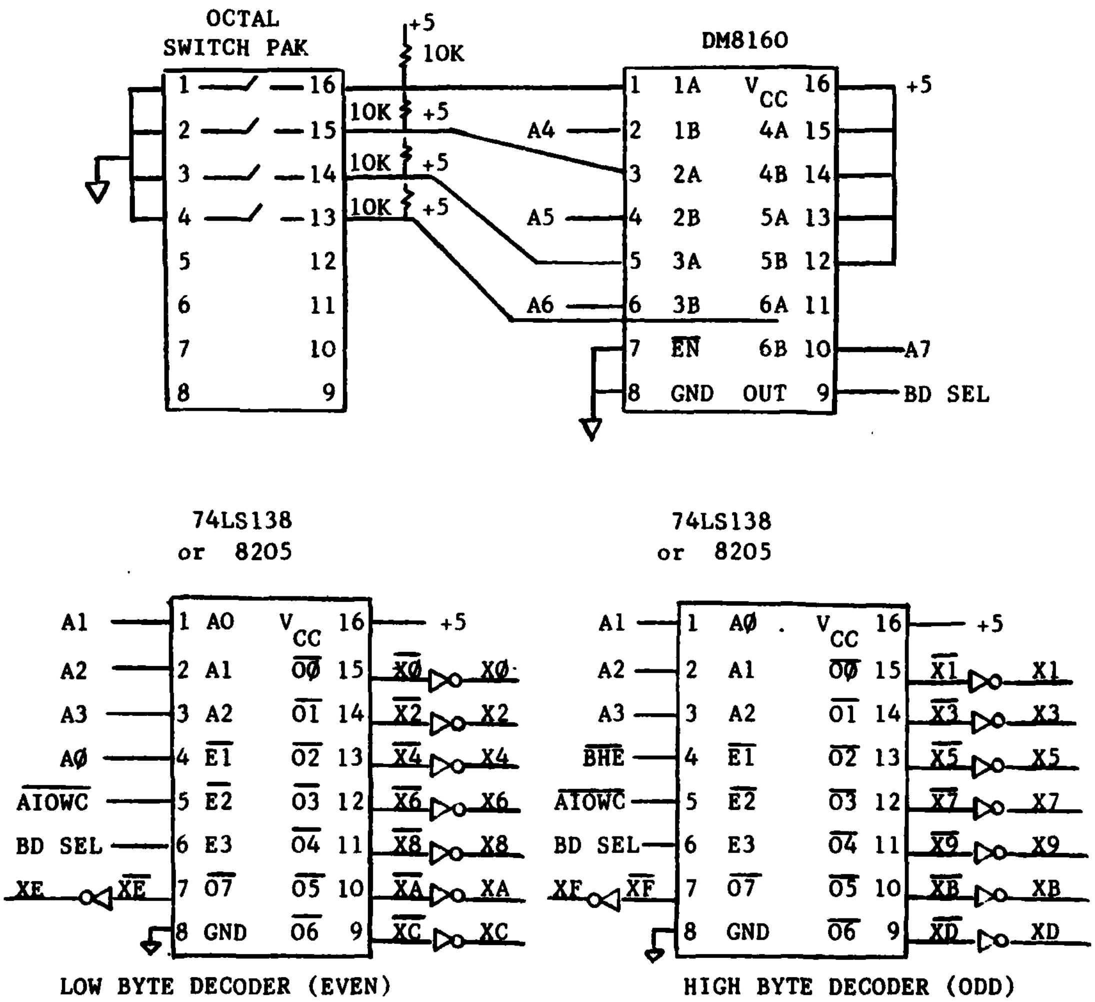
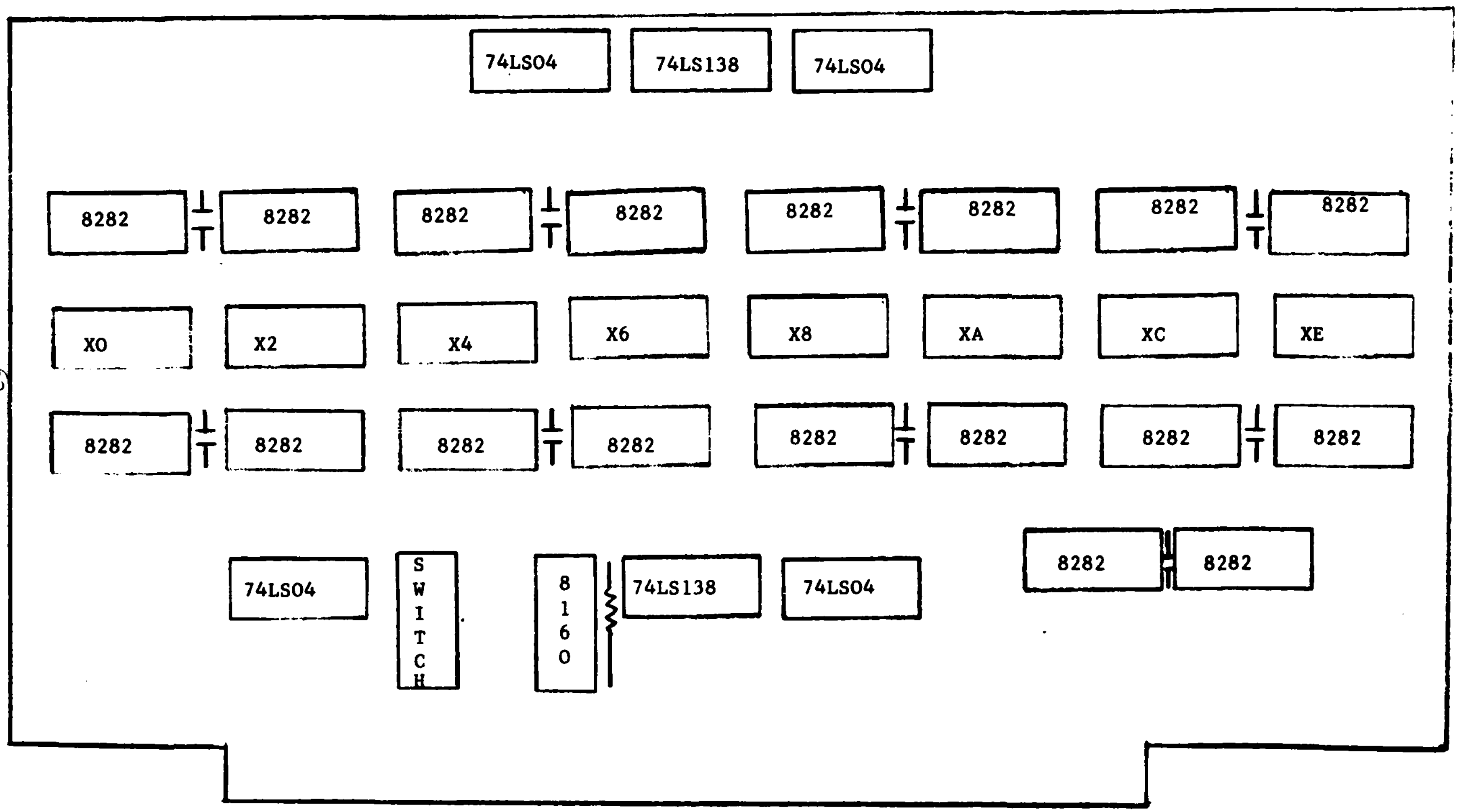


FIGURE 51. PARALLEL OUTPUT PORT DECODING



PARALLEL OUTPUT BOARD
FIGURE 52

BUFFERING

The output ports are buffered from the data bus to reduce noise and loading. The configuration of the output port buffers is shown in Figure 53. These IC's are connected as buffers and are always enabled and directed away from the system data bus.

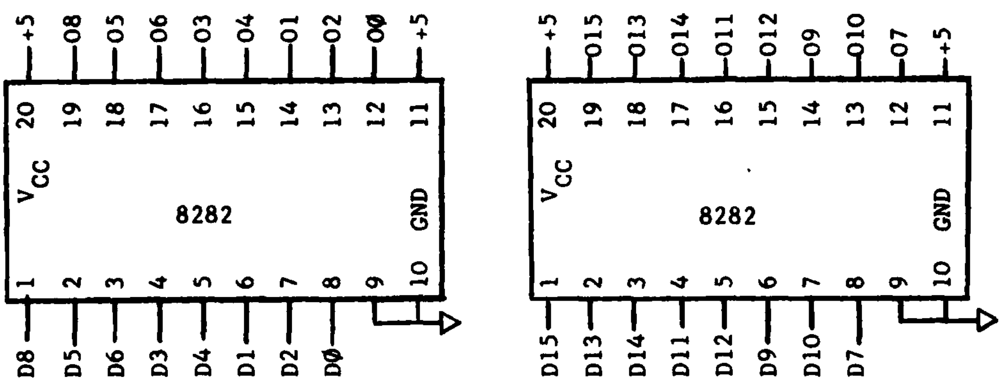


FIGURE 53. OUTPUT BOARD DATA BUS BUFFERS

THE PORTS

The ports consist of two 8282's used as latches. The 8282's tristate capability is continuously enabled. Figure 54 shows the configuration of an actual port.

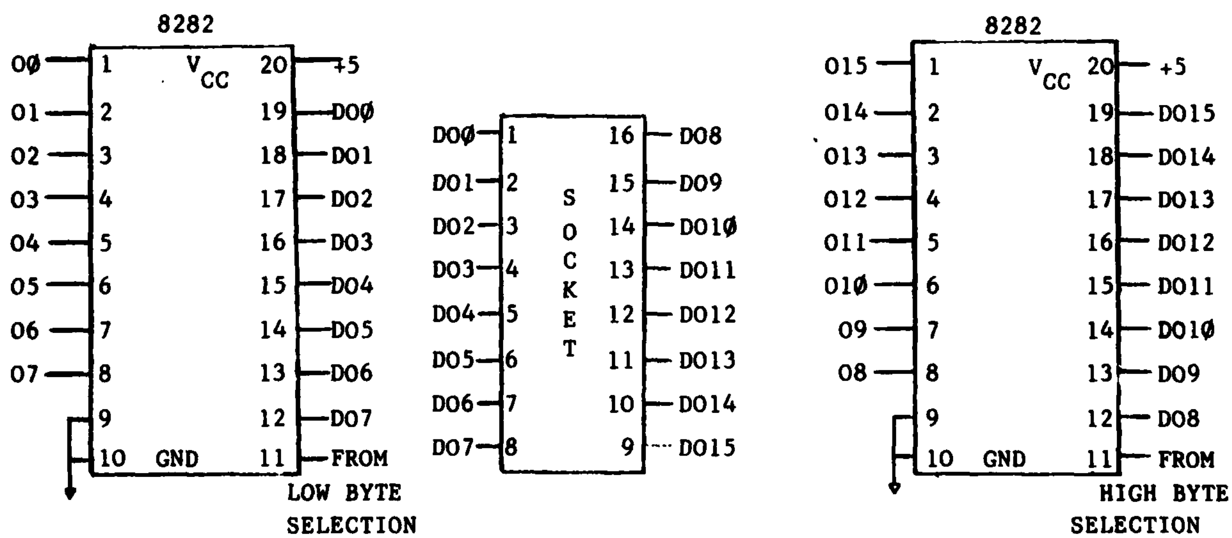


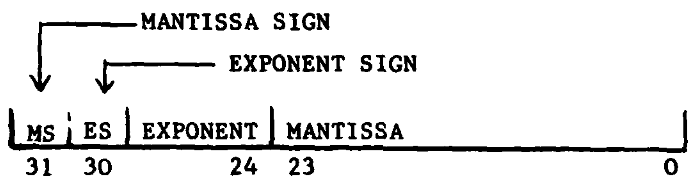
FIGURE 54. OUTPUT PORT CONFIGURATION

Analysis of the 8282's drive capability shows it is capable of sourcing -5ma on a logic 1 (2.4v) and sinking 32ma on a logic 0 (.5v). This is equivalent to a drive capability of 20 TTL loads.

VIII. THE ARITHMETIC PROCESSING BOARD

General Background

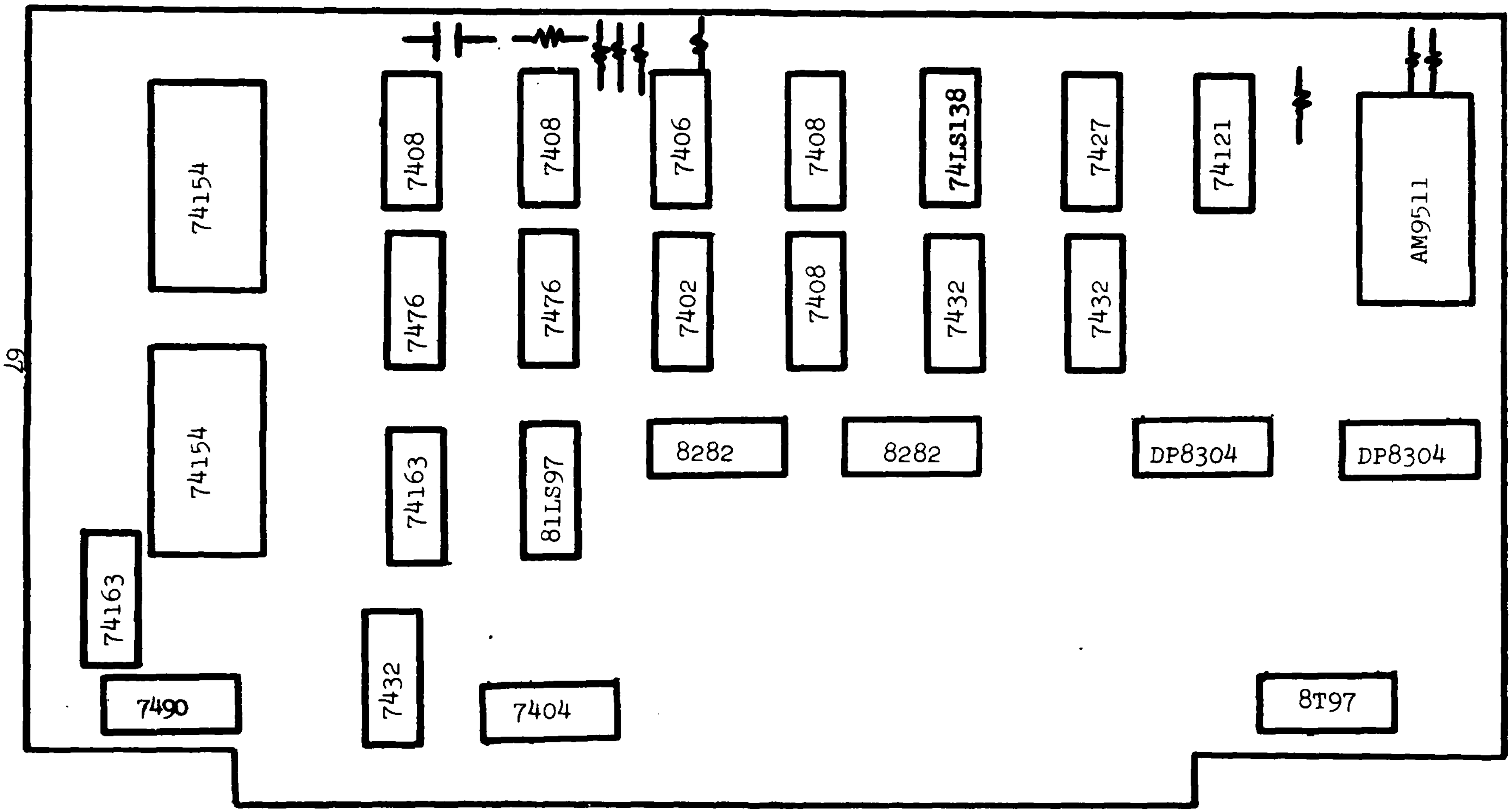
The arithmetic processing board of the USAFA/8086 is based on the Advanced Micro Devices 9511 arithmetic processing unit (APU). The APU is capable of 32 bit floating point functions as well as 16 and 32 bit two's complement integer arithmetic (13). The AM9511 at the time of the original system device was (and still is) the only microprocessor compatible arithmetic processing unit available. It is now second sourced by Intel Corporation. However, the manufacturer's original claim for a 4MHz capable unit has still to be met. If it is ever produced it will be possible to use the faster IC by minor modification of the existing system. The AM9511 uses the following floating point format:



The exponent is represented in two's complement format while the mantissa is in signed magnitude. In the 8086 system it is essential that all floating point words be located on boundaries evenly devisable by four (i.e., an address of XXXX0, XXXX4, XXXX8, or XXXXC) in order to be compatible with the hardware controller described in this chapter which is used for automatic data transfer with 8086's memory.

Automatic Data Transfer Controller

The arithmetic processing board (Figure 55) contains a counter-based automatic controller which can, given an address, transfer 4 sequential bytes of data either to or from the AM9511 APU. It is shown in block form



ARITHMETIC PROCESSOR UNIT
FIGURE 55

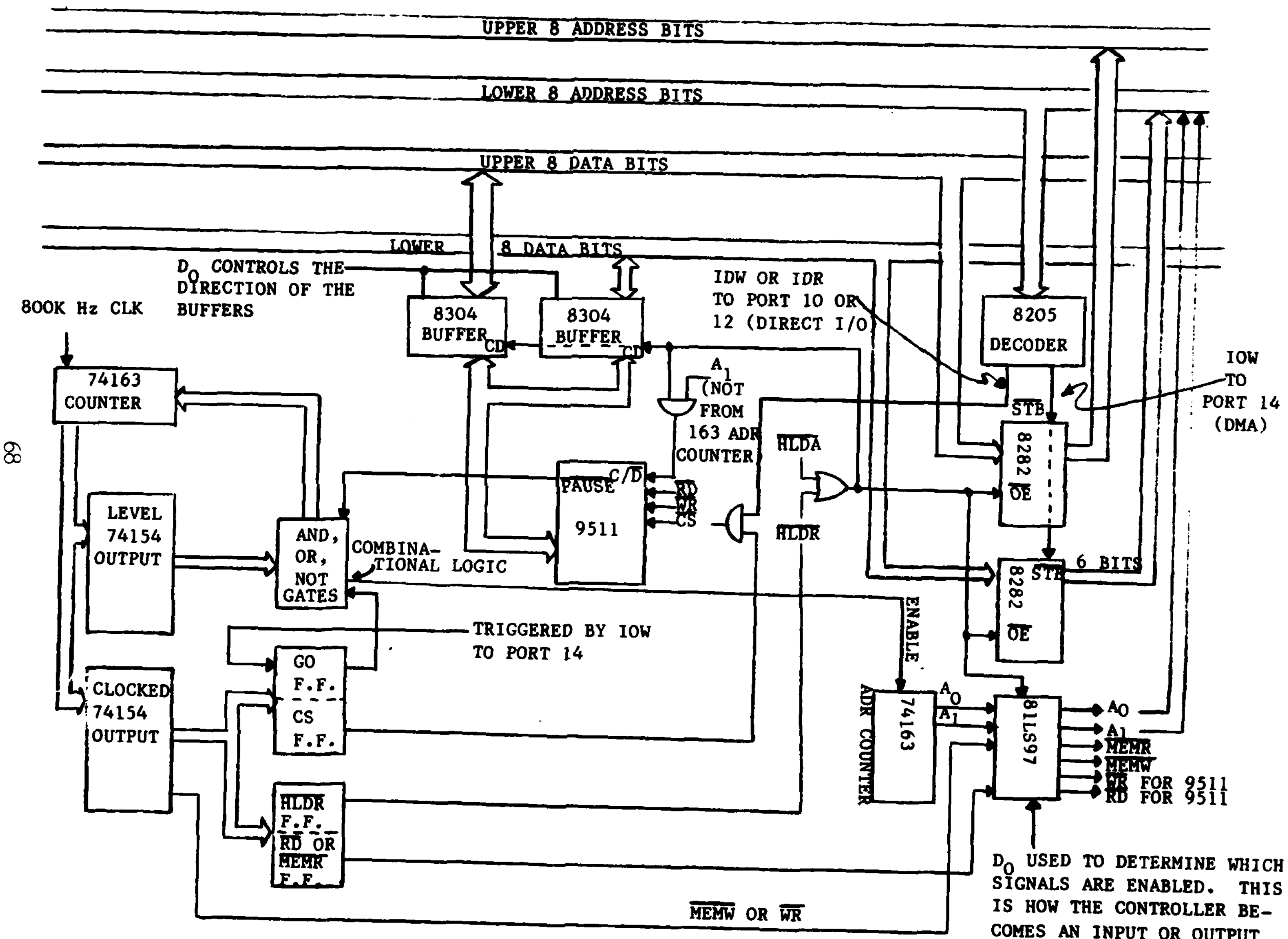


FIGURE 56. APU CONTROLLER BLOCK DIAGRAM

in Figure 56. This controller runs at a basic frequency of 800KHz which is derived from the 4MHz CPU clock as shown in Figure 57.

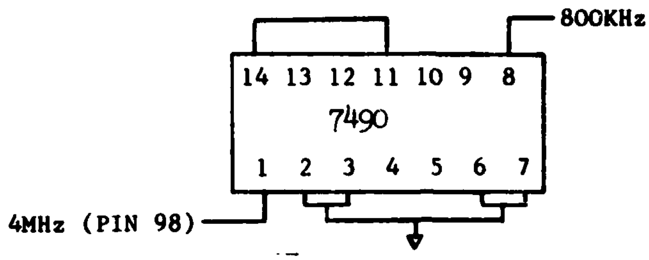


FIGURE 57. 800KHZ CLOCK GENERATION

The 800KHz clock then is used to drive a 74163 four bit binary counter which serves as the state controller for the system. This counter in turn drives two 74154 decoders which provide the clocked and level outputs of the controller as shown in Figure 58.

The four flip flops shown are used to generate control signals which must last longer than one clock cycle. The "Go" flip flop will remain set from the time the processor requests a transfer until the transfer is completed. The HLDR (Hold Request) flip flop requests use of the system bus through the CPU hold controller as described in Chapter IX. The CS flip flop (Chip Select) generates the required chip select for the AM9511 while either a read or write cycle takes place. The RD/WR flip flop enables the appropriate control signals to allow data transfers. If the transfer is from memory to the AM9511 then MEMR and WR to the 9511 must be used; otherwise, the RD of the 9511 and MEMW are appropriate. The method of selecting the appropriate set of signals is shown in Figure 59. The selection is based on the LSB of the requested transfer address. If it is given as an odd address, then

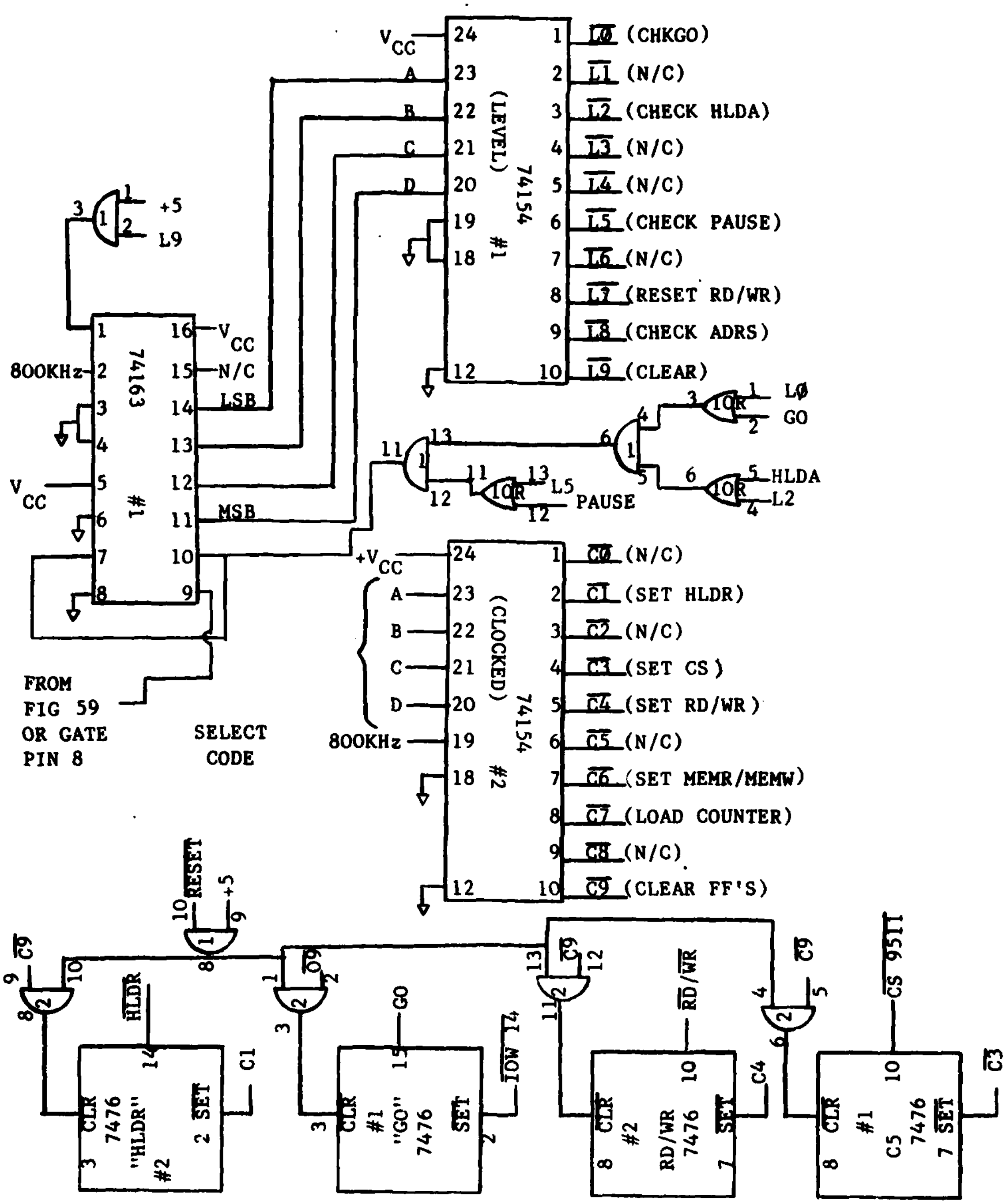
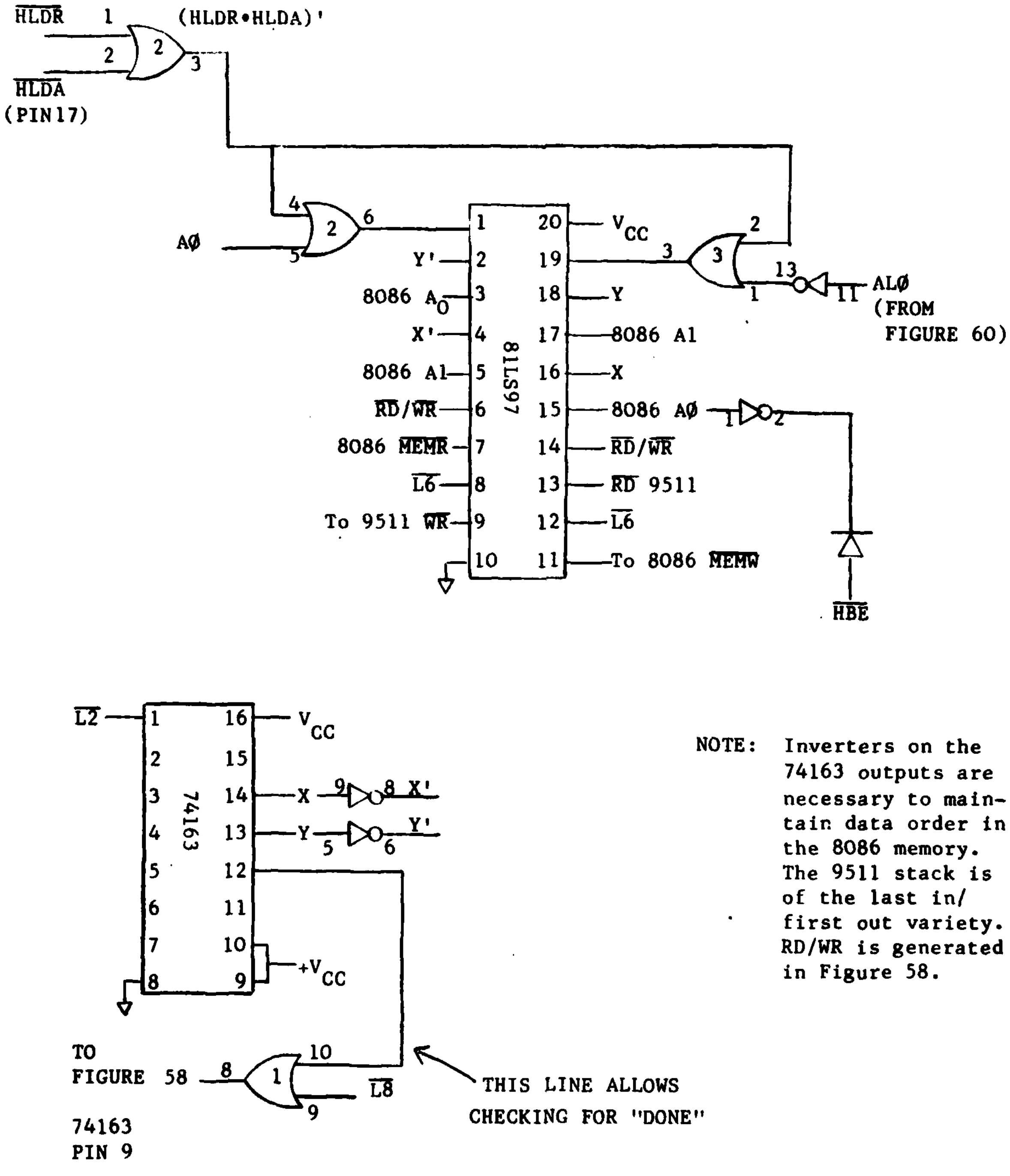


FIGURE 58. APU BASIC CONTROL COMPONENTS



NOTE: Inverters on the 74163 outputs are necessary to maintain data order in the 8086 memory. The 9511 stack is of the last in/ first out variety. RD/WR is generated in Figure 58.

FIGURE 59. APU CONTROL TRANSFER LOGIC

selection of the controller is accomplished by direct I/O to port 14. Figure 60 shows the decoding circuitry and address saving latches. All data is assumed to be in segment "0000". The 8T97 also provides the direct I/O (devices 10, 12) capability for the AM9511.

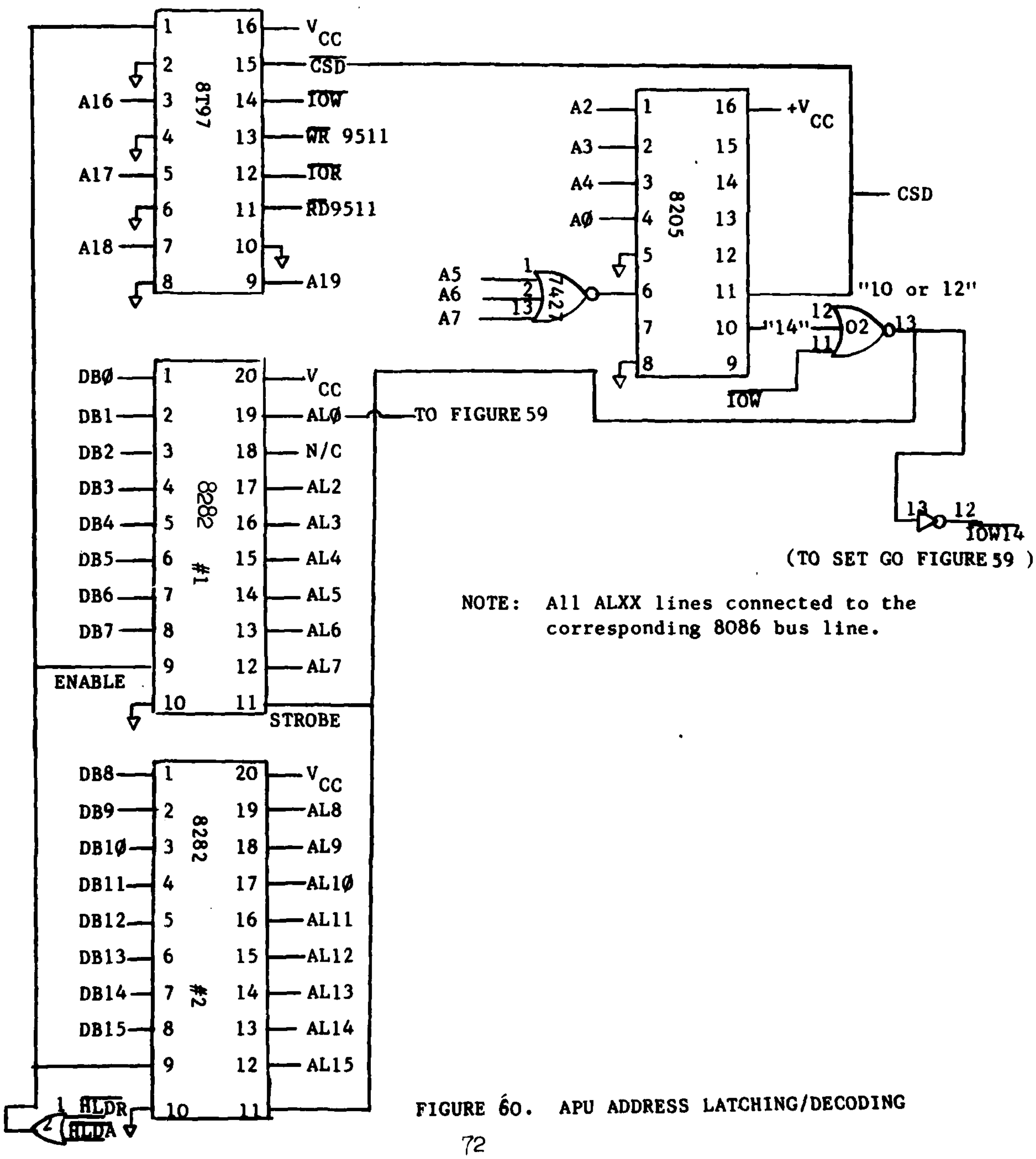
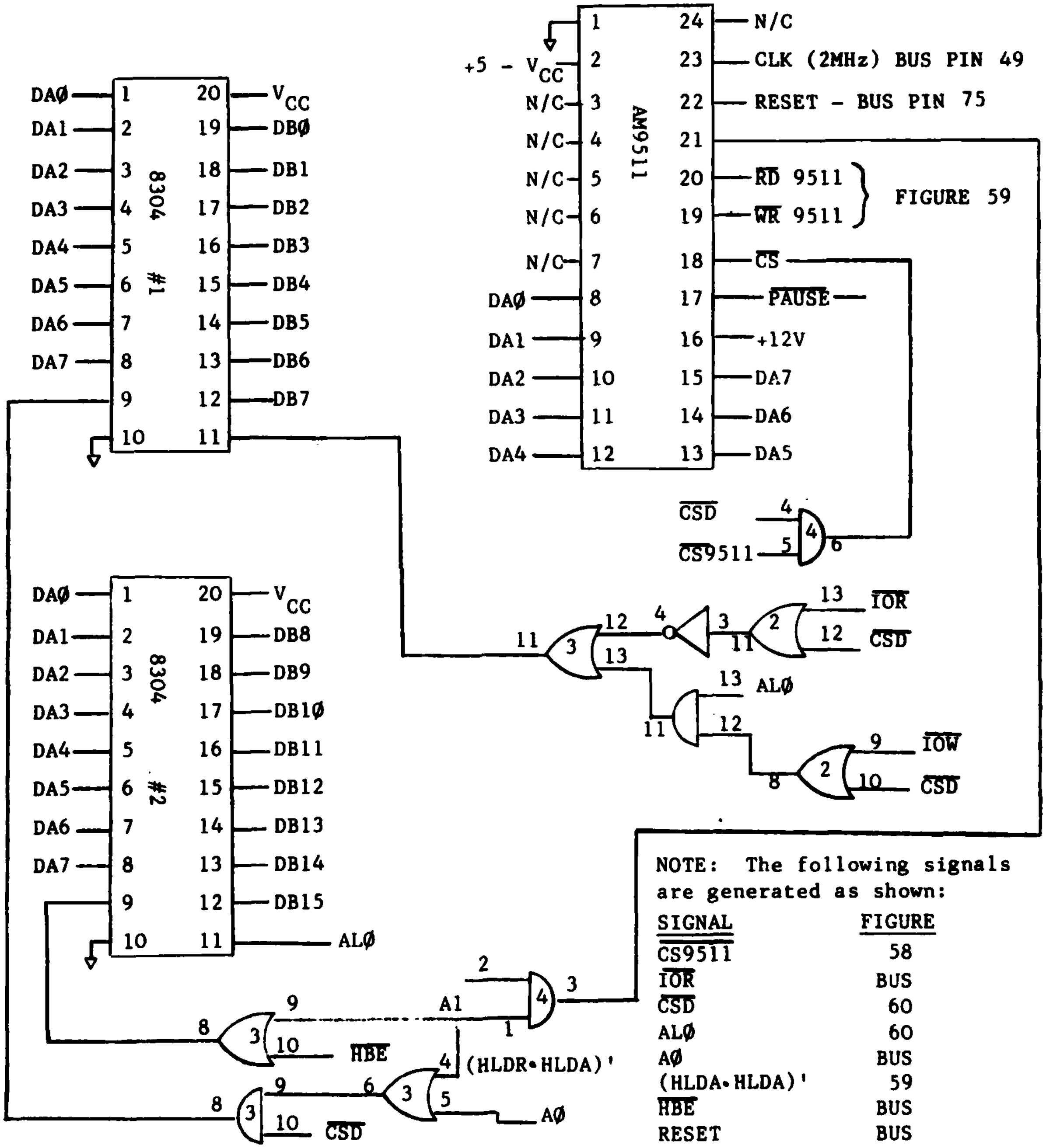


FIGURE 60. APU ADDRESS LATCHING/DECODING

Since the APU is essentially an 8 bit I/O device, the data must be transferred in 8 bit bytes. Figure 61 shows the circuitry including the AM9511.



NOTE: The following signals are generated as shown:

SIGNAL	FIGURE
$\overline{\text{CS9511}}$	58
$\overline{\text{IOR}}$	BUS
$\overline{\text{CSD}}$	60
ALØ	60
AØ	BUS
(HLDA•HLDA)'	59
$\overline{\text{HBE}}$	BUS
RESET	BUS
CLK (2MHz)	BUS
$\overline{\text{IOW}}$	BUS

FIGURE 61. DATA TRANSFER CIRCUITRY

Since we are using a 2MHz AM9511 it is necessary to slow the processor down through use of the RDY line when data is read from or written to the APU. The processor itself (after learning of the requested action) may then additionally slow the CPU drive through use of its $\overline{\text{PAUSE}}$ line. Figure 62 shows the appropriate circuitry. Recall the $\overline{\text{RDY}}$ line is an open collector technology line.

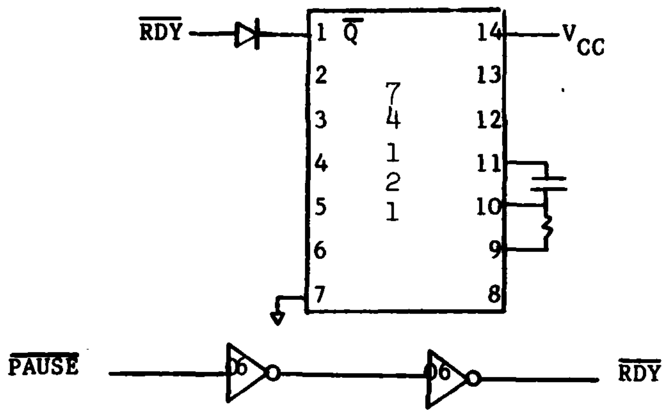


FIGURE 62. DELAY CIRCUITRY APU

The following pages contain an English description of the operations designed into the APU controller. Figure 63 shows the overall state diagram of the system.

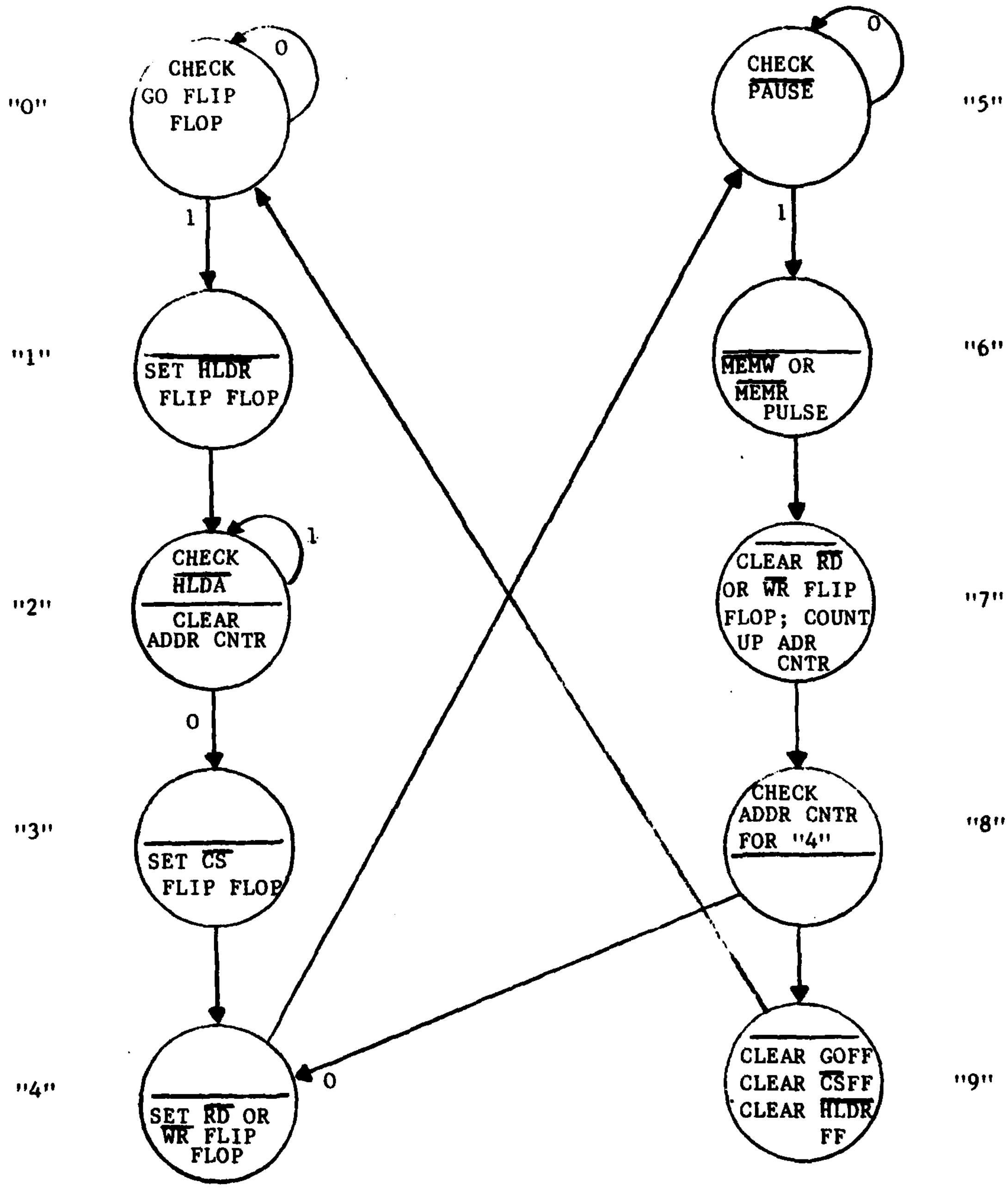


FIGURE 63. APU CONTROLLER STATE DIAGRAM

State 0

In this state the "GO" flip flop is checked to see if it has been set. This flip flop will be set whenever the 8205 decoder decodes a 14 on the lower 8 address lines and an IOW is issued. Since the same controller performs both the input and output, we must tell it which one it is to do. This is accomplished in this state with the use of the least significant data bit. When DØ is a zero it will read from the 8086 (output) and when DØ is a one it will write to the 8086 (input).

State 1

A hold request (HLDR) is issued in this state. HLDR does not go directly to the 8086. The 8086 in the maximum mode does not respond to a level command on its $\overline{RT}/\overline{GT}$ ($\overline{\text{Request}}/\overline{\text{Grant}}$) line. Rather, the Hold Controller previously described on the CPU Board is used (Chapter IV).

State 2

In the second state the $\overline{\text{HLDA}}$ line is checked. The $\overline{\text{HLDA}}$ tells the APU controller it can use the bus. Also, all buffers are enabled and the $C/\overline{D}$ line will go low. Additionally, the address counter that controls the two least significant bits of the address when writing or reading from memory is cleared.

State 3

State 3 issues a chip select ($\overline{\text{CS}}$) to the AM9511. This tells the AM9511 that the APU controller wants to talk to it.

State 4

In this state, the flip flop that actually issues a read or write is set. Depending on whether the controller is doing an output or input, the flip flop's signal will go to the $\overline{WR}$ or $\overline{RD}$ line on the AM9511. A two-sided buffer (81LS97) is used to control the $\overline{RD}$ and $\overline{WR}$ command. One side of the buffer contains the signals for an output ($\overline{RD}$ command issued) and the other side contains the signals for an input ($\overline{WR}$ command issued). Each side can be enabled separately. DØ determines which side is enabled as discussed under State Ø.

<u>State 5</u>

The $\overline{PAUSE}$ line from the AM9511 is checked in this state. This line goes low when a read is requested. It will return high when the data bus from the AM9511 contains valid data. This line also remains low if a previously issued command has not been completed. In either case the data bus is not valid until the $\overline{PAUSE}$ line goes high.

<u>State 6</u>

The $\overline{MEMR}$ or $\overline{MEMW}$ pulse is issued in this state. Again, which signal is issued depends on which side of the 81LS97 is enabled. The memory read or write signal is one of the clocked outputs from a 74154.

<u>State 7</u>

The flip flop that issues the $\overline{RD}$ or $\overline{WR}$ to the AM9511 is reset. This has to be done because the stack inside the AM9511 only rotates each time a new $\overline{RD}$ or $\overline{WR}$ command is issued. The address counter that gives the APU controller the capability to read or write from four consecutive memory locations is counted up.

<u>State 8</u>

A check is made of the address counter. If it is not a four then a jump is made to state 4. Once the address counter has reached four then the DMA controller has written to or read from four memory locations and is done. It then goes to State 9.

State 9

State 9 resets all the flip flops. This takes the $\overline{CS}$ away from the AM9511 and also $\overline{HLDR}$ goes high. $\overline{HLDR}$ going high tells the CPU Hold controller to issue a third pulse on the $\overline{RT}/\overline{GT}$ line telling the 8086 it can have its bus back. At the same time the counter for the APU controller is cleared and returns to State Ø.

DIRECT I/O TO AM9511

Direct I/O is the easiest way to access the AM9511. This capability is needed to issue commands to the AM9511. The interface is easy and not complicated.

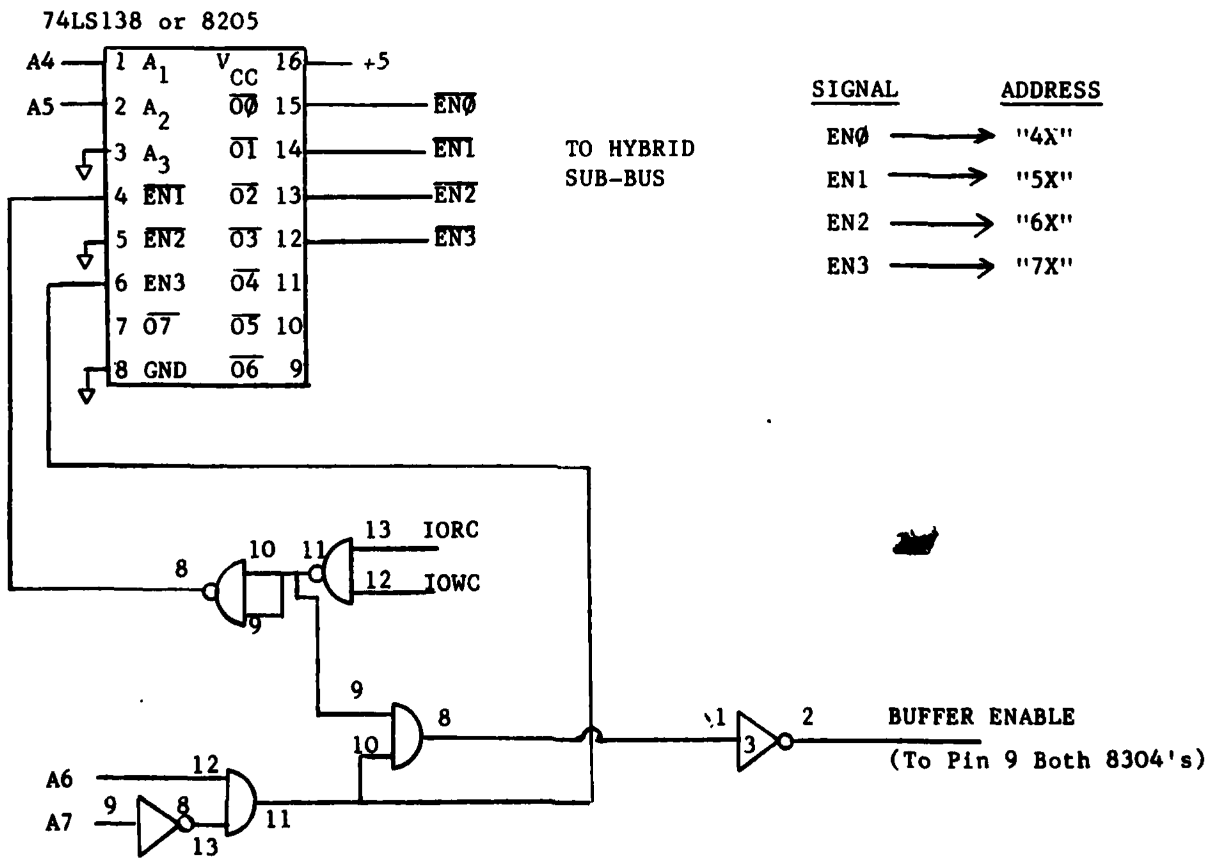
The direct I/O uses ports 10 and 12. An 8205 decodes the lower 8 address buts and provides the $\overline{CS}$ to the AM9511. The A1 line is connected to the $C/\overline{D}$ line on the AM9511. Port 12 is used for commands. The $\overline{IOR}$ and $\overline{IOW}$ lines from the 8086 are used to tell the AM9511 whether to read or write to its stack. All these commands go through combinational logic with the APU controller to insure no conflicts arise between the two.

IX. HYBRID INTERFACE BOARD

The hybrid interface board in addition to providing signal buffering for those signals distributed to the hybrid sub-bus also contains the system timers (8253), their associated clocks (1MHz, 100KHz, and 10KHz), the system USART (Universal Synchronous/Asynchronous Receiver Transmitter), and its associated baud rate generator. Figure 65 shows a general overview of the board.

Decoding For The Hybrid Sub-Bus

To minimize the decoding for each card on the hybrid sub-bus the signals ENØ, EN1, EN2, and EN3 are created on the hybrid interface board. These signals indicate an IOWC or IORC has been issued to a device residing on the sub-bus. The circuitry used is shown in Figure 64.



SIGNAL		ADDRESS
ENØ	→	"4X"
EN1	→	"5X"
EN2	→	"6X"
EN3	→	"7X"

FIGURE 64. HYBRID SUB BUS SELECTION LOGIC

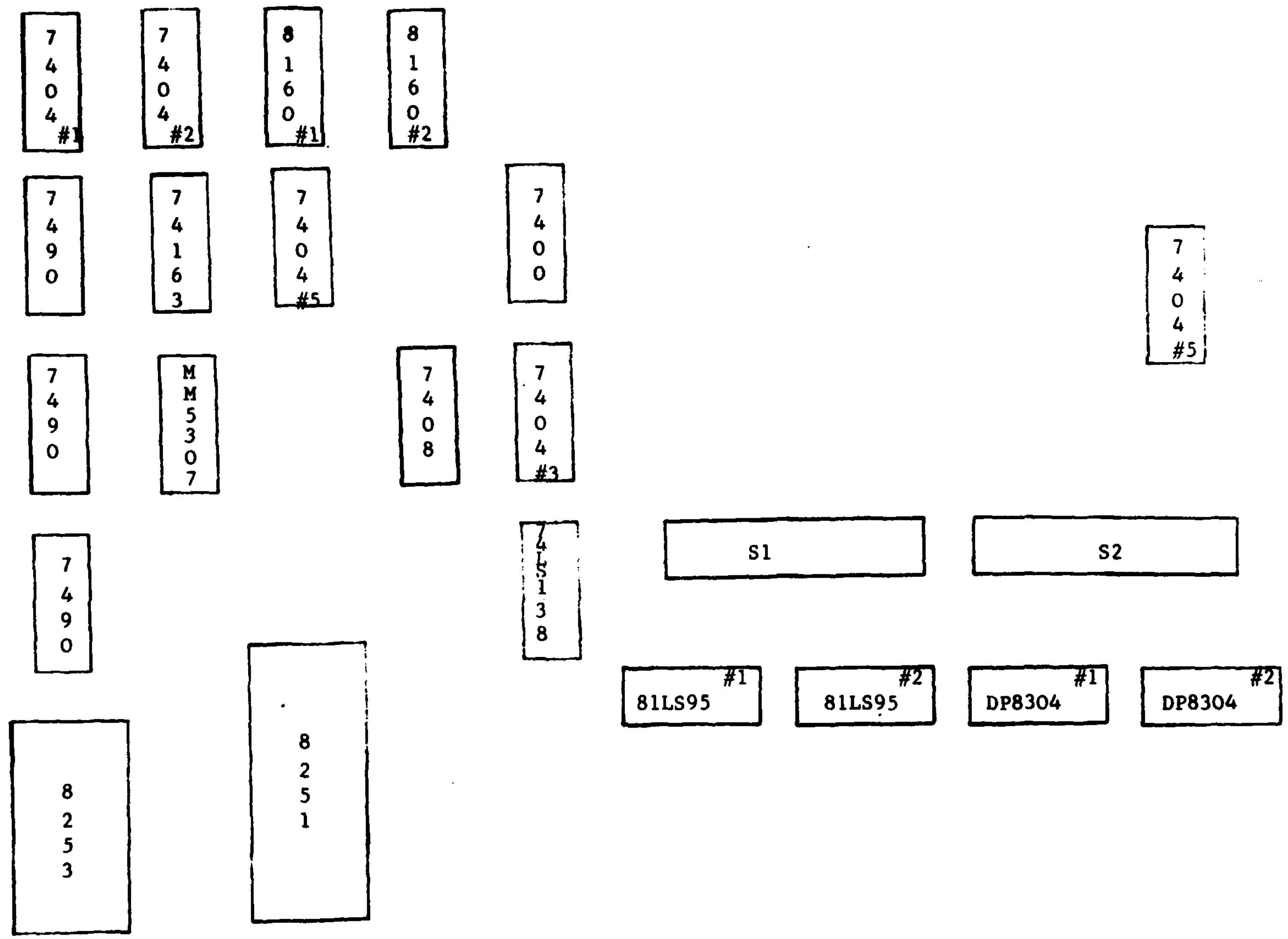
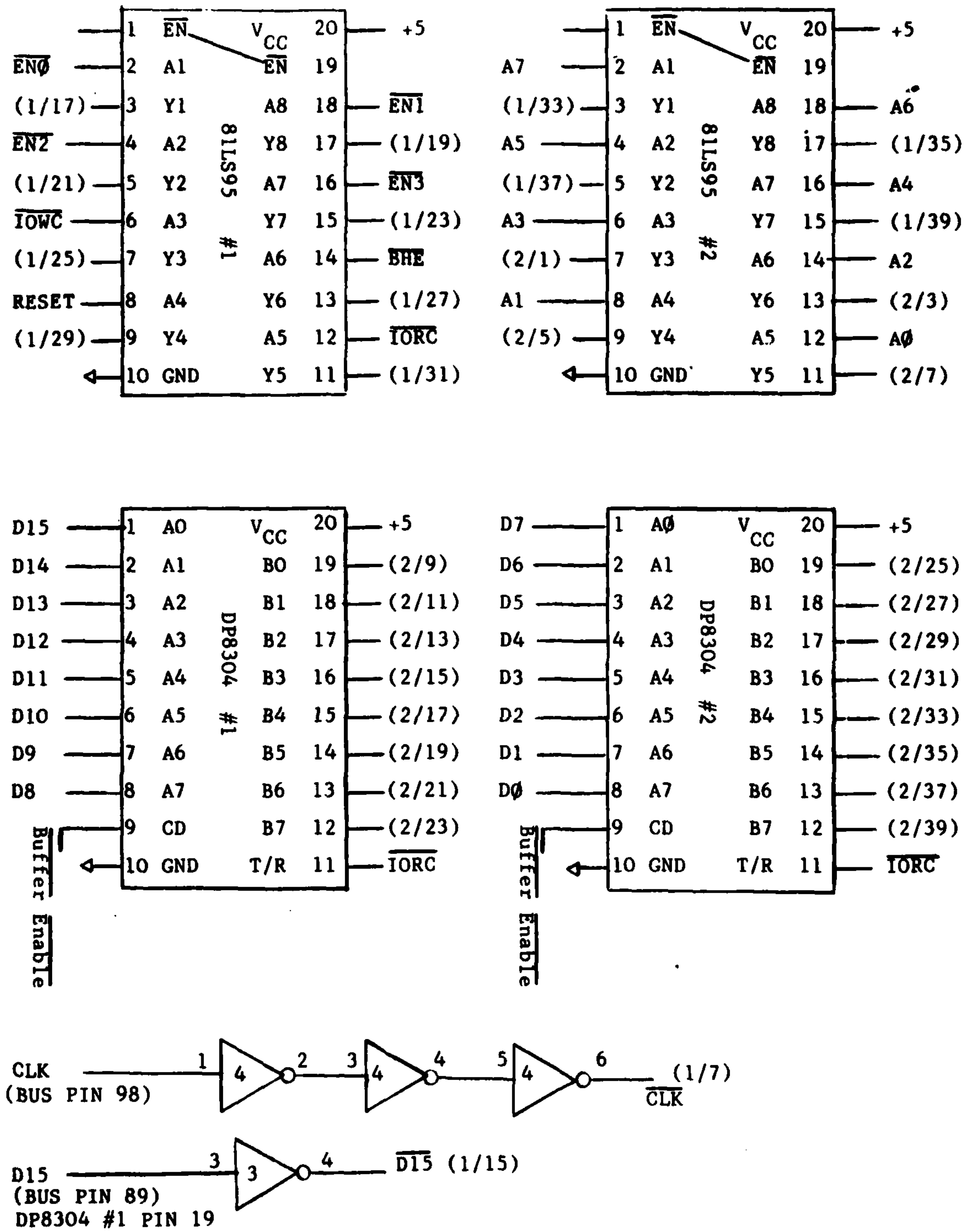


FIGURE 65
HYBRID INTERFACE CARD TOP SIDE VIEW

Data Buffering For The Hybrid Sub-Bus

The data bus is buffered using two DP8304's while the address and control signals are buffered using 81LS95's. The unidirectional 81LS95's are continuously enabled. 81LS97's are suitable substitutes for the application. The DP8304's are enabled using the decoding shown in Figure 66. The direction of these buffers is controlled using the $\overline{\text{IORC}}$ line directly off the bus. Hence, these buffers normally face toward the sub-bus and are reversed whenever an $\overline{\text{IORC}}$ is executed. The data buffers and connections to the 40 pin cable pair used to interconnect with the sub-bus are all listed in order in Table 9, 8086 Bus to Hybrid Sub-Bus Cabling. At the sub-bus end the two 40 pin cables are terminated and interfaced to the sub-bus through a 44 pin Vector wirewrap card according to the assignments of Table 9 and repeated in order in Table 10.



NOTATION: (1/39)⟹(CONNECTOR/PIN); ALL EVEN # PINS ARE GROUNDED.

FIGURE 66. HYBRID SUB BUS DATA BUFFERING

TABLE 9

8086 BUS TO HYBRID SUB BUS CABLING

8086 INTERFACE S1	SIGNAL	HYBRID INTERFACE CARD	8086 INTERFACE S2	SIGNAL	HYBRID INTERFACE CARD
1	N/C		1	A3	A
3	N/C		3	A2	B
5	N/C		5	A1	C
7	$\overline{\text{CLK}}$	V	7	A0	S
9	N/C		9	D15	15
11	N/C		11	D14	14
13	N/C		13	D13	P
15	$\overline{\text{D15}}$ (Out Only)	R	15	D12	13
17	$\overline{\text{EN0}}$	5	17	D11	N
19	$\overline{\text{EN1}}$	E	19	D10	12
21	$\overline{\text{EN2}}$	6	21	D9	M
23	$\overline{\text{EN3}}$	F	23	D8	11
25	$\overline{\text{IOWC}}$	D	25	D7	L
27	$\overline{\text{BHE}}$	16	27	D6	10
29	RESET	19	29	D5	K
31	$\overline{\text{IORC}}$	4	31	D4	9
33	A7	T	33	D3	J
35	A6	17	35	D2	8
37	A5	U	37	D1	H
39	A4	18	39	D0	7

BUS CONNECTIONS AT BACK PLANE OF SUB BUS

1	+100	Y	ANA COM
2	+15	Z	ANA COM
3	+5	19,W	DIG GND
21	-15	20,X	DIG GND
22	-100		

TABLE 10
8086 SUB BUS FOR HYBRID OPERATIONS

COMP SIDE

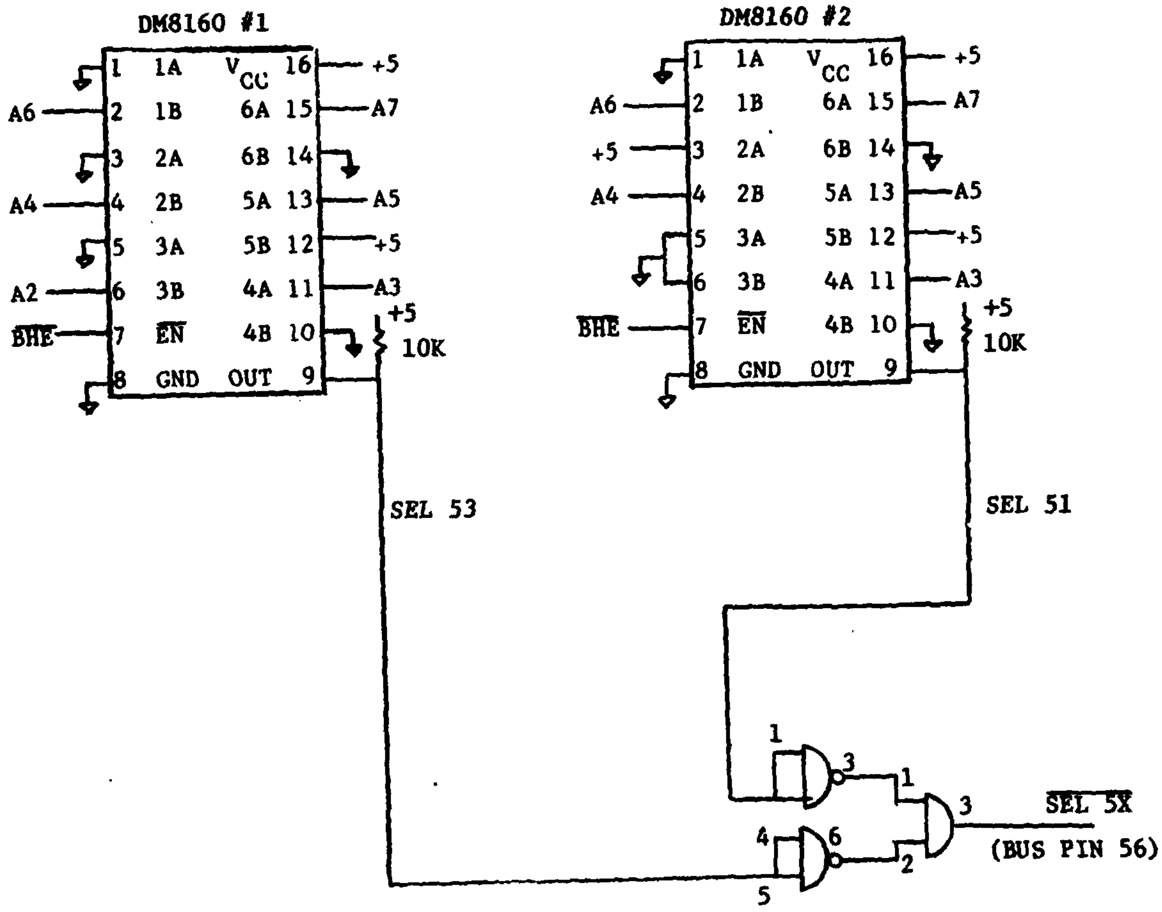
1	+100
2	+15
3	+5
4	$\overline{\text{IORC}}$
5	$\overline{\text{EN1}}$
6	$\overline{\text{EN3}}$
7	DØ
8	D2
9	D4
10	D6
11	D8
12	D10
13	D12
14	D14
15	D15
16	$\overline{\text{BHE}}$
17	A6
18	A4
19	DIG GND
20	DIG GND
21	-15
22	-100

WIRING SIDE

A	A3
B	A2
C	A1
D	$\overline{\text{IOWC}}$
E	$\overline{\text{EN2}}$
F	$\overline{\text{EN4}}$
H	D1
J	D3
K	D5
L	D7
M	D9
N	D11
P	D13
R	D15*
S	AØ
T	A7
U	A5
V	$\overline{\text{CLK}}$
W	DIG GND
X	DIG GND
Y	ANA COM
Z	ANA COM

Decoding For The USART and Timers

Two 8160's are used to decode selection of the system USART and the timer. As delivered the USART is at "21_H" and "23_H". The timer is at "31_H", "33_H", "35_H", and "37_H". Figure 67 shows the configuration of the comparators.



Pins 1,3,5,10,12, and 14 are strapped according to the desired device address.

FIGURE 67. - USART/TIMER DECODING

The SEL5X signal is used by the CPU card to delay I/O operations with the USART and timer and thus extend the access time allowed by the 8086.

USART Circuitry

The USART Circuitry consists of the 8251 itself as well as those IC's associated with the baud rate generator. Figure 68 details the circuitry. Three inverters are interconnected to form an 8.2944 MHz TTL oscillator. This signal is then sent through a module-9 counter leading to a 44% duty cycle 921KHz TTL clock which drives the MM5307 baud rate generator. By changing the strapping on pins 8, 9, 10, and 11 of this IC according to the device specification baud rate is selectable from 50 to 19200 baud. The USART is a very versatile programmable LSI device whose characteristics are discussed in (6:63) and (12:12-46). The diode resistor pair used at the output of the MM5307 limit the baud rate clock to acceptable TTL levels. Prior to sending and receiving data with the 8251, the data is double buffered on the hybrid interface board to increase drive capability and protect the LSI circuit.

Timer Circuitry

The 8253 contains three extremely versatile timers capable of being operated in 5 different modes (12:12-65). The supporting circuitry for this device consists of TTL compatible clock generation at 1MHz, 100KHz, and 10KHz. Figure 67 shows the timer connections and its support circuitry. Provision is made on the hybrid interface board to jumper the timer outputs to the system interrupts. Timer ϕ (Device 31) runs at 10KHz. Timer 1 (Device 33) uses 100KHz and Timer 2 (Device 35) runs at 1MHz.

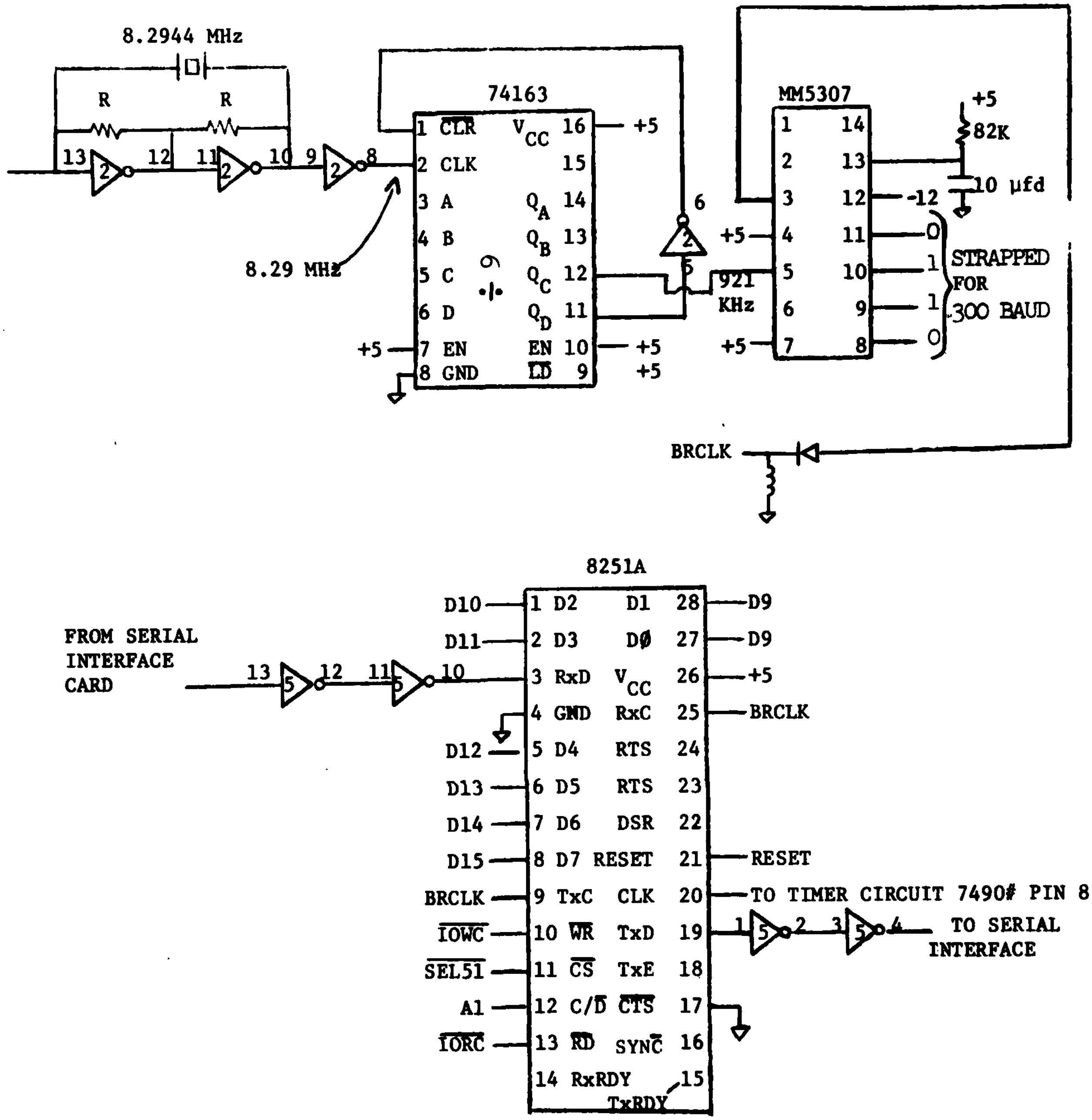


FIGURE 68. USART CIRCUITRY

AD-A091 772 AIR FORCE ACADEMY CO F/G 9/2
THE USAFA/8086 - A STATE OF THE ART MICROPROCESSOR SYSTEM. VOLU--ETC(U)
JUN 80 J J POLLARD
UNCLASSIFIED USAFA-TR-80-16-VOL-1 NL

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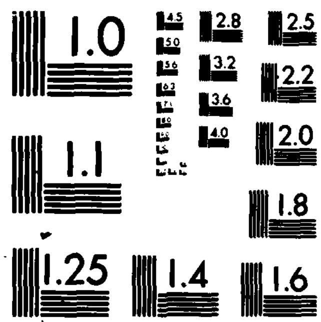

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0

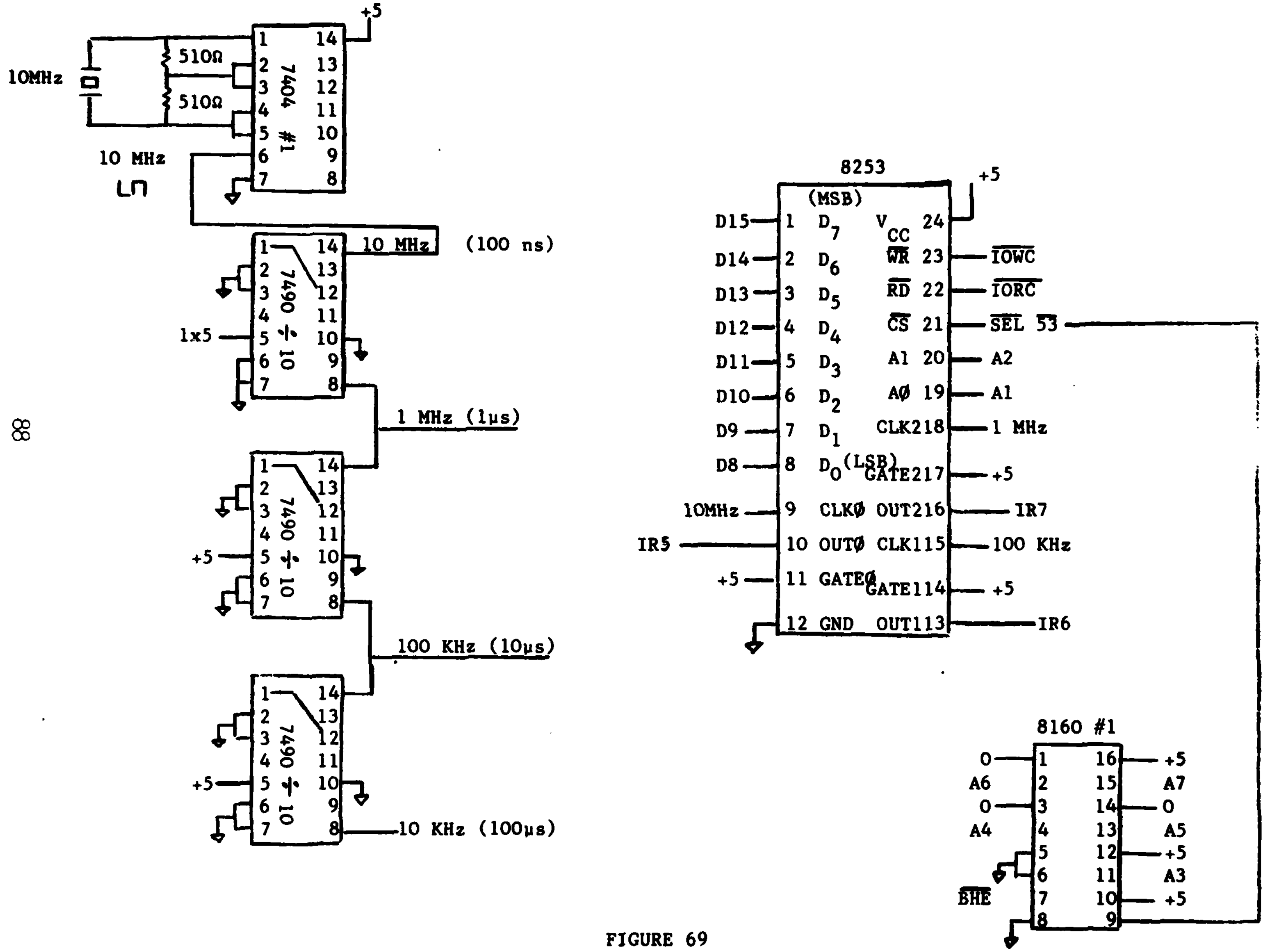


FIGURE 69
HYBRID INTERFACE: TIMER CIRCUITRY

IX. SERIAL INTERFACE BOARD

The serial interface card is designed to provide a multipurpose serial interface between any TTL input/output UART/USART circuit and standard serial I/O devices. The interface is capable of handling a 20 ma current loop as used with a teletype, an RS-232 level (±12 volt) inverted logic terminal such as the TI Silent 700 series of machines, and finally an inverted logic buffered TTL level as sometimes used in telemetry operations.

The 20 ma Loop

The 20 ma circuit is an opto isolated circuit utilizing the 4N33 which is capable to 30KHz. The input circuit used is shown in Figure 70 .

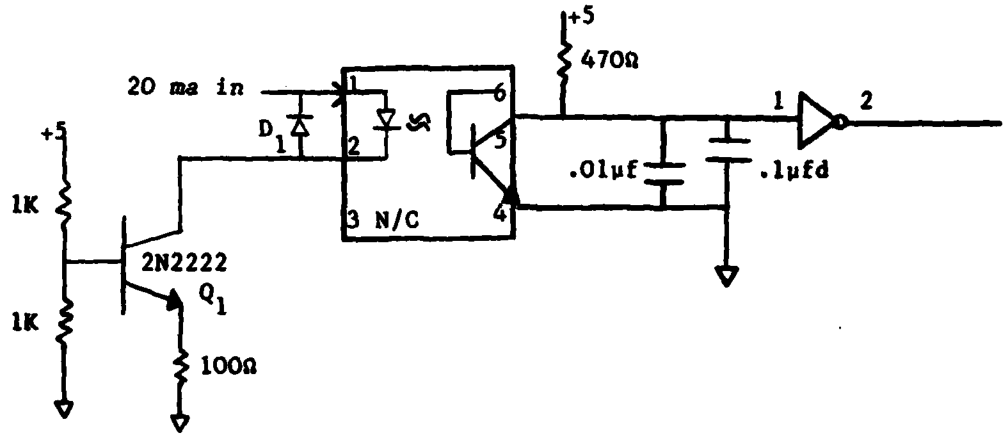


FIGURE 70. 20ma LOOP INPUT CIRCUITRY

Diode D_1 suppresses negative voltage spikes induced in data transmission. Current enters the anode of the LED in the 4N33 causing light to turn on the Darlington transistor pair of the 4N33. The current out of the LED is limited by transistor Q_1 to approximately 20ma. The output stage of the 4N33 is pulled up to 5 volts to provide TTL compatible levels. The capacitors serve as noise filters. Since, when the LED is on, the transistor in the 4N33 is on causing the output to go to near zero volts, it is necessary to invert the output for proper logic level transmission to the

UART/USART. The output circuit used is shown in Figure 71.

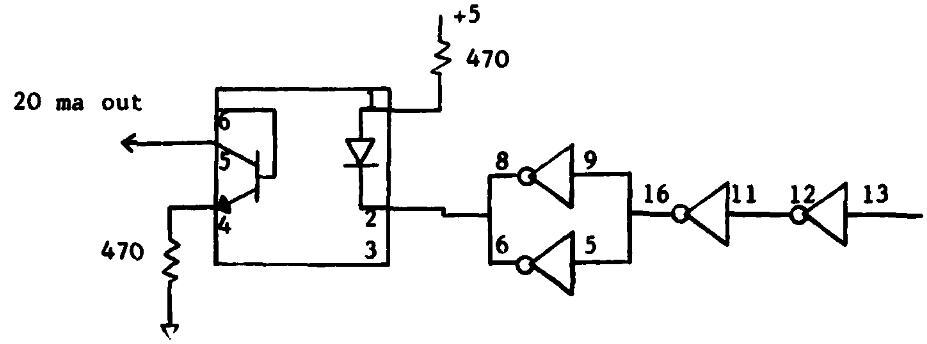


FIGURE 71. 20ma LOOP OUTPUT CIRCUITRY.

When the logic gate connected to the 4N33 LED asserts a "zero" current is drawn through the LED causing the Darlington transistor pair to be turned on. Current will then be sunk by the transistor pair through the 470Ω emitter follower resistor. If 12 volts is used as the source, about 25ma will be drawn. A standard TTY connector is supplied with the interface. It is connected as shown in Figure 72. No paper tape support circuitry is provided.

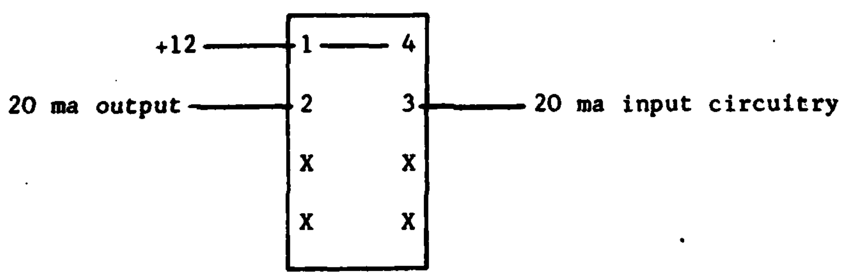
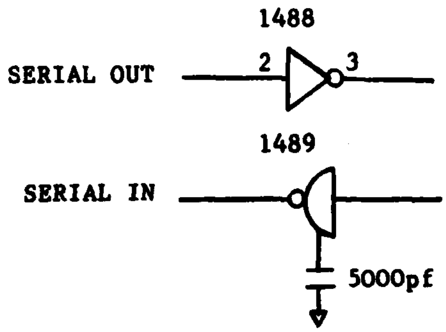


FIGURE 72. TTY CIRCUITRY

RS-232 Level Circuitry

The RS-232 level circuitry is implemented directly using the MC1488/1489 (75188/75189) pair of level shifters. The circuits used are shown in Figure 73. Since RS-232 transmissions are inverted logic transmissions, these circuits suffice as shown. DB25S/P connectors are used to interface the RS-232 levels. Pin-out is given in Figure 76.



SIGNAL	PIN#
	2
	3
SIGNAL GROUND	7

FIGURE 73. RS-232 LEVEL SHIFTING CIRCUITRY

Inverted TTL Level Interface

Inverted TTL level inputs/outputs are also provided by the circuitry below. Utilizing the 7438 gives high circuit drive capability.

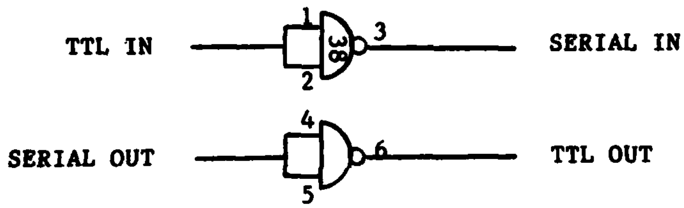


FIGURE 74. TTL LEVEL OUTPUTS

Pin Selectable Options

Since the various input signals are not compatible a single jumper is on the card to allow selection between 20ma loop, RS-232, and TTL.

O 20ma

O RS-232 O Serial In

O TTL

FIGURE 75. INPUT SELECTION

2 - Transmitted Data

3 - Received Data

7 - Signal Ground

FIGURE 76. DB25 RS 232 CONNECTOR

X. THE HYBRID SUBSYSTEM

The hybrid subsystem consists of an interface for connecting signals needed to and from the main system bus, an eleven slot 44 pin card edge sub bus, 8 dual channel Digital to Analog Converter cards, and a two card 16 channel Analog to Digital Conversion system. The hybrid subsystem port for port is the most expensive sub-system in the USAFA/8086.

The Sub Bus Interface Card

This wire-wrapped card merely transitions from the two 40 pin cables used for signal transmission from the main system bus through the hybrid interface board to the 44 pin sub-bus. The interconnections are detailed in Chapter IX, Table 10. The sixteen system data lines are pulled up (terminated) on the sub-bus interface card. No power is transmitted through the 40 pin cables. All sub-bus power is provided through separate supplies connected at the sub-bus itself.

The Dual Channel D/A Card

The dual channel D/A card consists of a pair of identical circuits which are shown in block diagram form in Figure 77. The position of these components on the actual card is shown in Figure 78.

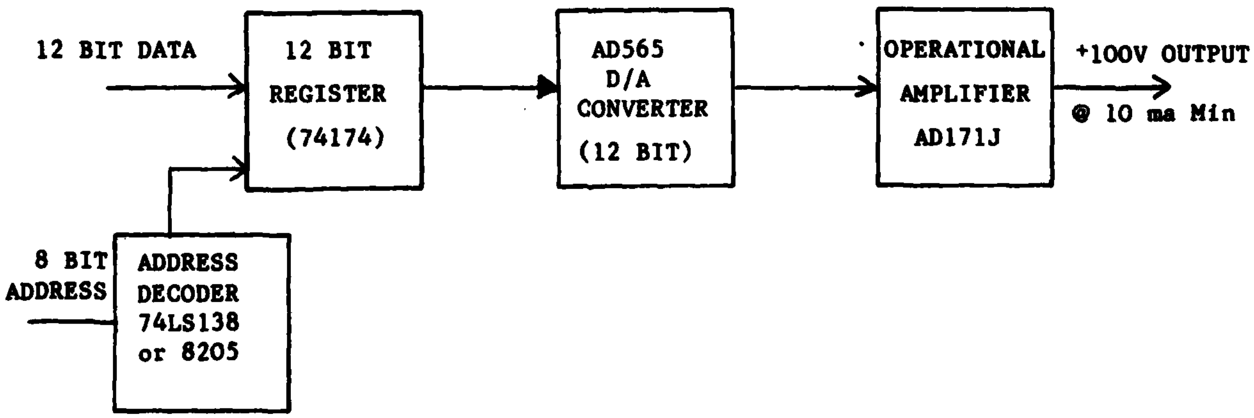


FIGURE 77. BLOCK DIAGRAM D/A CHANNEL

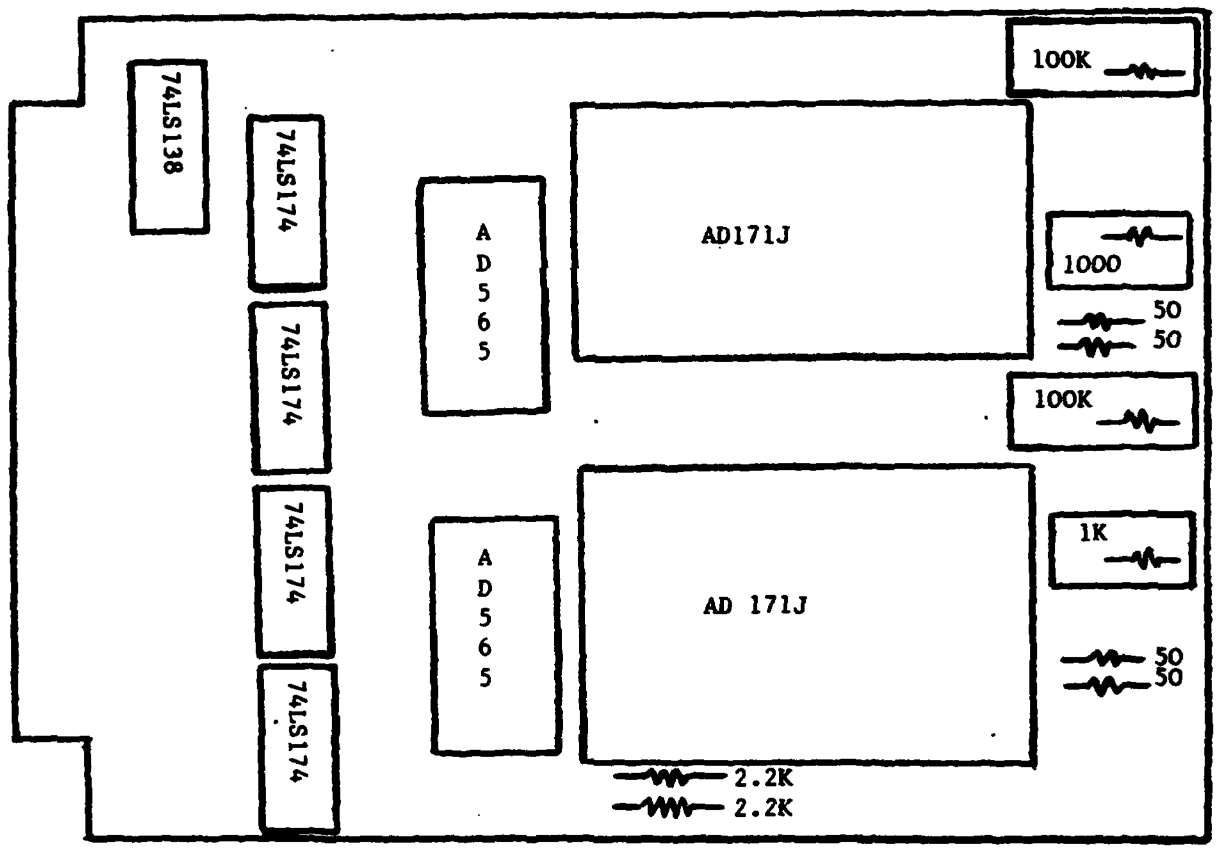


FIGURE 78
DUAL CHANNEL D/A BOARD

Figure 79 shows the configuration of the actual components used in the system. The AD565 is detailed in Reference (14). The AD171J is specified in Reference (15).

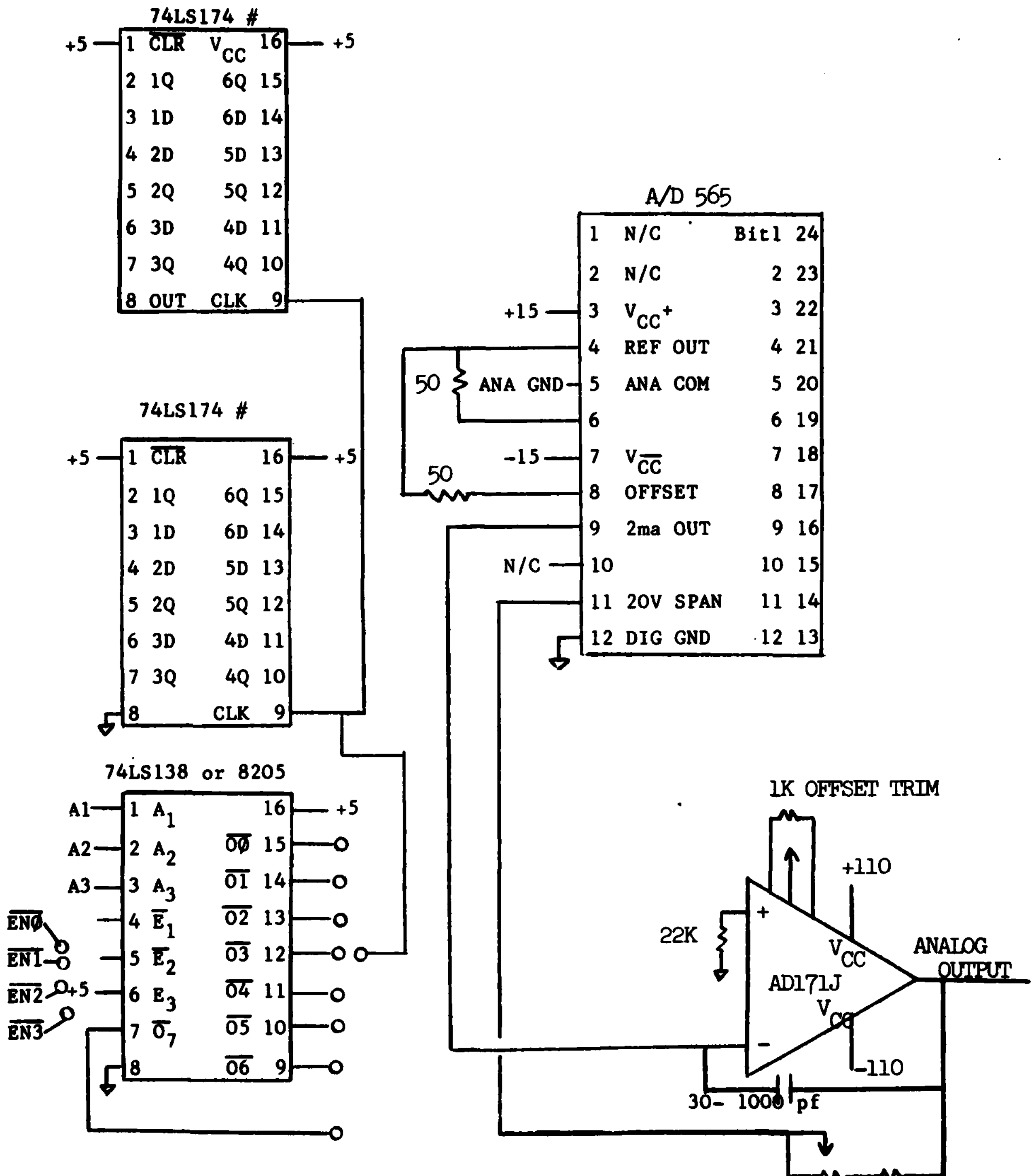


FIGURE 79. D/A BOARD CONNECTIONS

The Analog to Digital Conversion System

The analog to digital conversion system used in the USAFA/8086 consists of two printed circuit boards. The first of these is a counter-based controller and cache memory which allows the automatic continuous sequential conversion of all sixteen analog channels. The second board is basicly analog in nature and prepares and converts each of the sixteen analog channels. Figures 80 and 81 show actual component positions on the two boards.

The Analog Board

The analog board consists of two 8:1 analog multiplexors, a sample/hold circuit, a high speed successive approximation converter and sixteen input scaling potentiometers. Figure 82 shows a block diagram of the analog board.

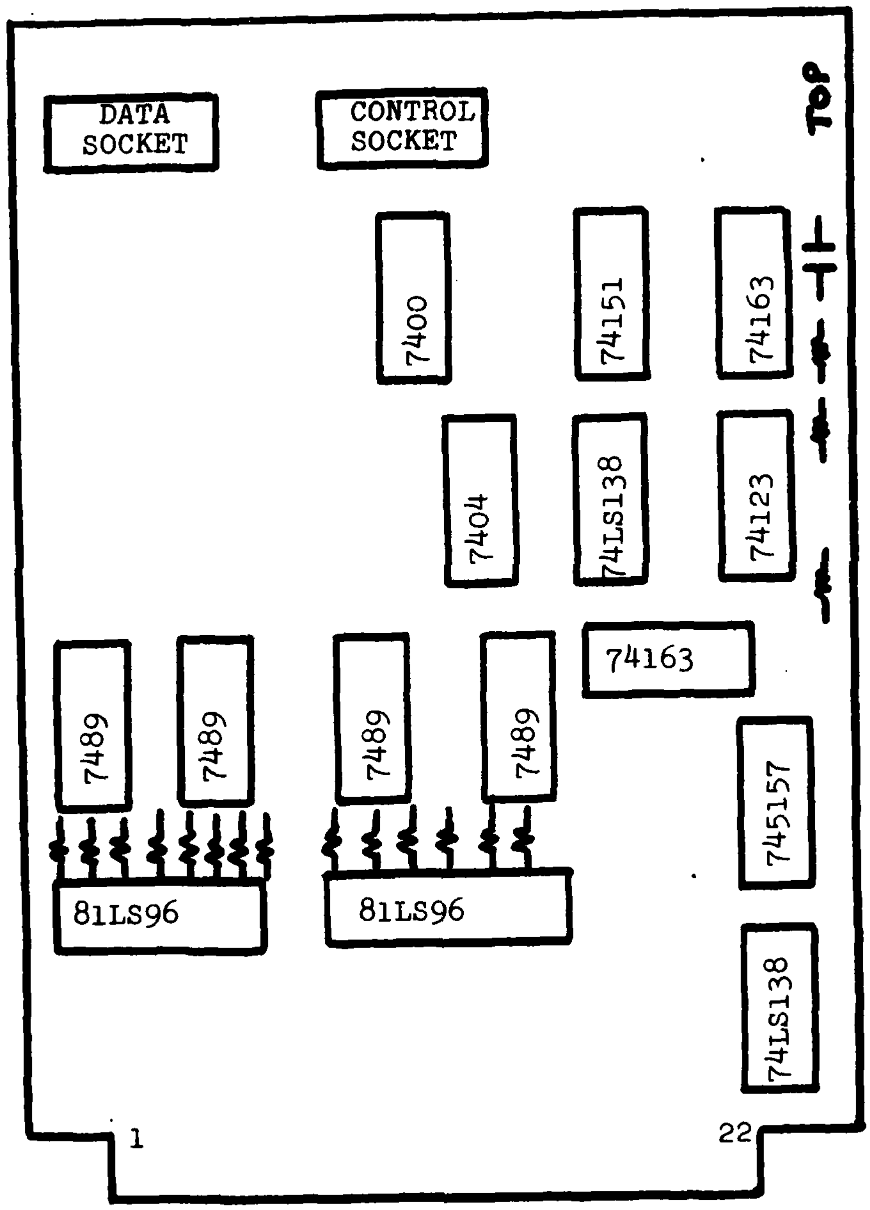


FIGURE 80. ANALOG/DIGITAL CONTROLLER BOARD

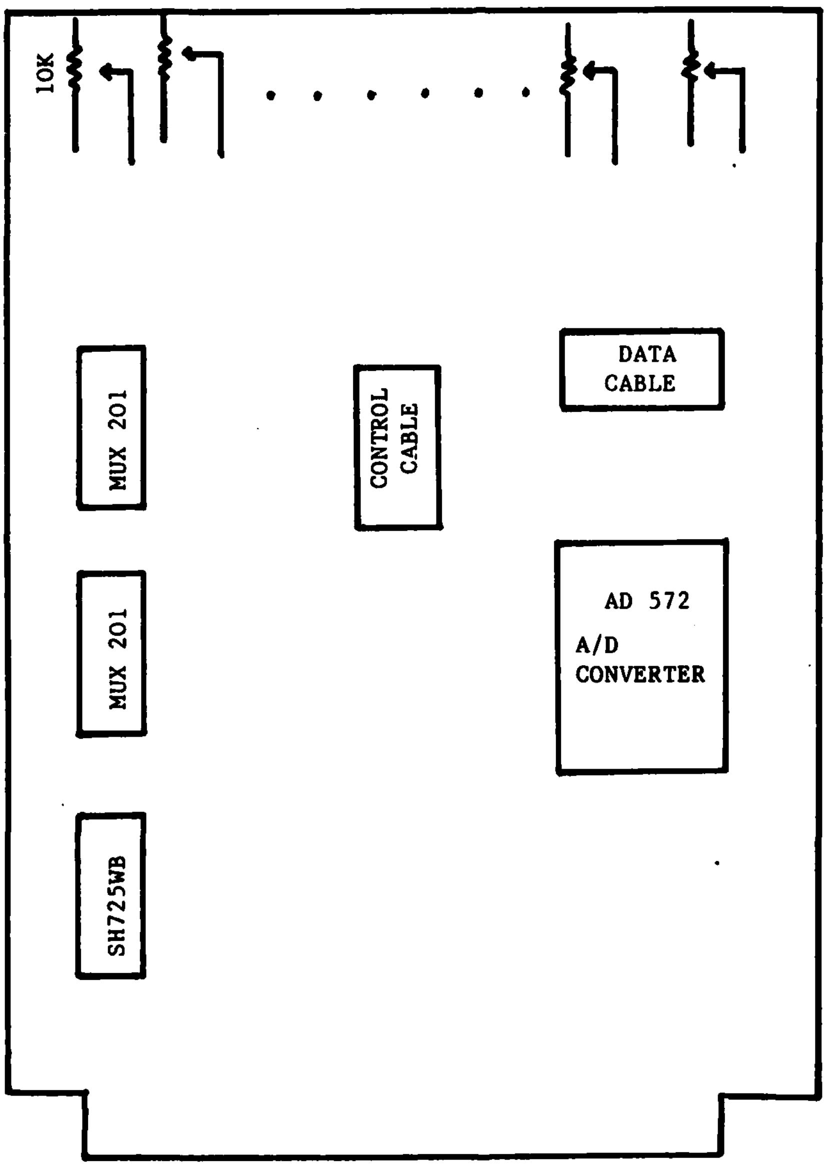


FIGURE 81. ANALOG DATA ACQUISITION BOARD

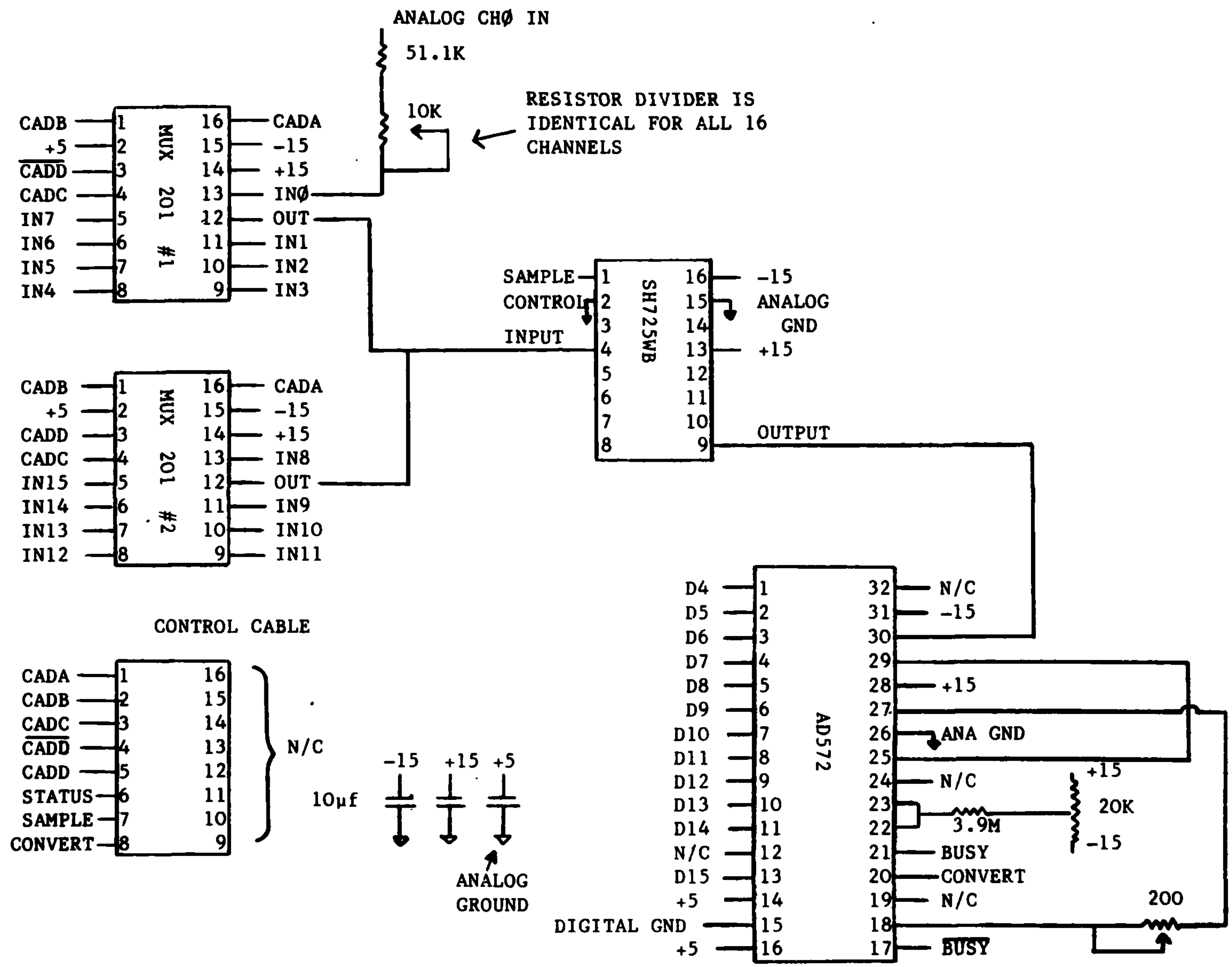


FIGURE 82. SCHEMATIC DIAGRAM OF ANALOG BOARD OF A/D SYSTEM

Analysis of the Analog Board

Several factors are essential in considering the throughput of the analog board.

a. The settling time (ts) through the mux to .01% of value is 1μs.

b. The acquisition time (ta) of the sample/hold circuit is 15μs.

c. The slew rate (tslew) of the sample/hold circuit is 3v/μs.

d. The droop rate of the sample/hold circuit is 5mV/ms.

e. The conversion time (tc) of the A/D converter is 25μs.

This implies that the time from selection of the analog value to digital value at a minimum should be considered to be:

$$T = t_s + t_a + \Delta V\ \mathrm{max}/3V\ \mu s + t_c$$

$$= 1 + 15 + 20/3 + 25\ \mu s$$

$$\approx 1 + 15 + 7 + 25\ \mu s = 48\ \mu s$$

For the 16 signal system, at best, the cycle time is 16x50μs = 800 μs. If we have one sample every 800μs we can theoretically reconstruct a signal of period 1600μs or 625 Hz. More realistically, a faithful reconstruction of signals of period 800μs should be considered or about 60Hz. This is based solely on analysis of the maximum analog throughput and will be degraded by some additional slight delays from the digital controller.

The input impedance of each analog channel is the value of the scaling resistor which was chosen to be at least 51K.

The Digital Board

The digital board implements the state diagram of Figure 83 utilizing a counter-based controller. At power on the counters (74163's) are reset to 0000 placing the controller in state 0 and addressing memory location zero. The controller checks to see a conversion is not currently in progress by checking the busy bit of the AD1131J previously discussed. If not, then it proceeds to update the memory address register (counter) for the on board 16 word by 16 bit cache memory created from high speed bipolar 7489 memories. The memory address register also serves as the analog channel selector.

In state 2 the controller stores the most recently acquired data by issuing a write pulse to the memory. In state three a sample pulse is transmitted to the SH725WB of 15μs duration. State four waits for the sampling process to be completed and then state five orders the new sample to be converted. The conversion pulse (200ns min, 400ns max) is verified in state six and we then progress through state seven back to state zero. This process continues repeatedly until stopped by the processor requesting data from the cache memory through an input request to ports 40 thru 5E. If the computer is requesting data the controller will be stopped at its next entry into state two. Writing will be inhibited to the cache memory until the process or request has been accomplished. To avoid conflict the computer is forced not ready for at least 5μs on each data request. This means it takes about 6μs to acquire the latest analog value of a given channel. If this operation was requested directly to the analog conversion system instead of to the controller, minimum data access time would have been 50μs as we have previously computed.

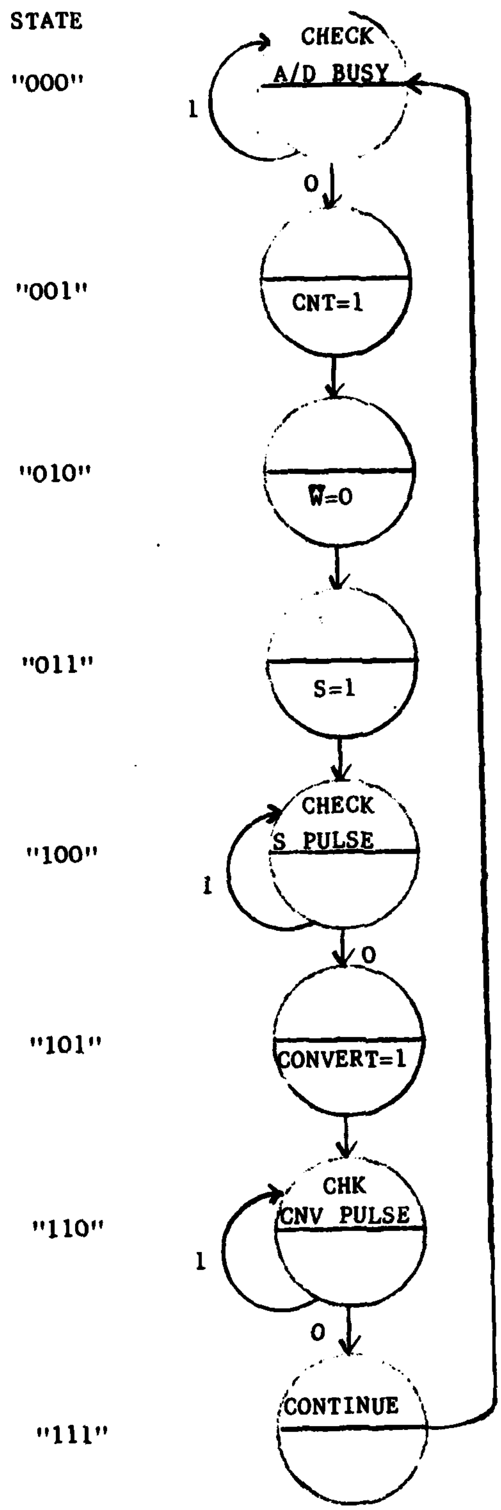


FIGURE 83
A/D STATE DIAGRAM

The actual hardware pinout is given in Figure 84. The 74163 #1 serves as the state counter. 74163 #2 is the address register. 74138 #1 is the level output decoder while 74151 serves as the controller input multiplexor. Two halves of a 74123 generate the sample and convert pulses. The 74657 selects the address ultimately reaching the cache memory of four 7489's between the controller generated address and the computer generated address. 74138 #2 detects computer requests and forwards them to the controller. The 81LS95's are tristate inverting buffers which interface the data lines to the sub-bus. The two least significant bits are always returned zero when a data request is made by the computer rounding out the sixteen bit data field from the twelve bits supplied by the A/D converter.

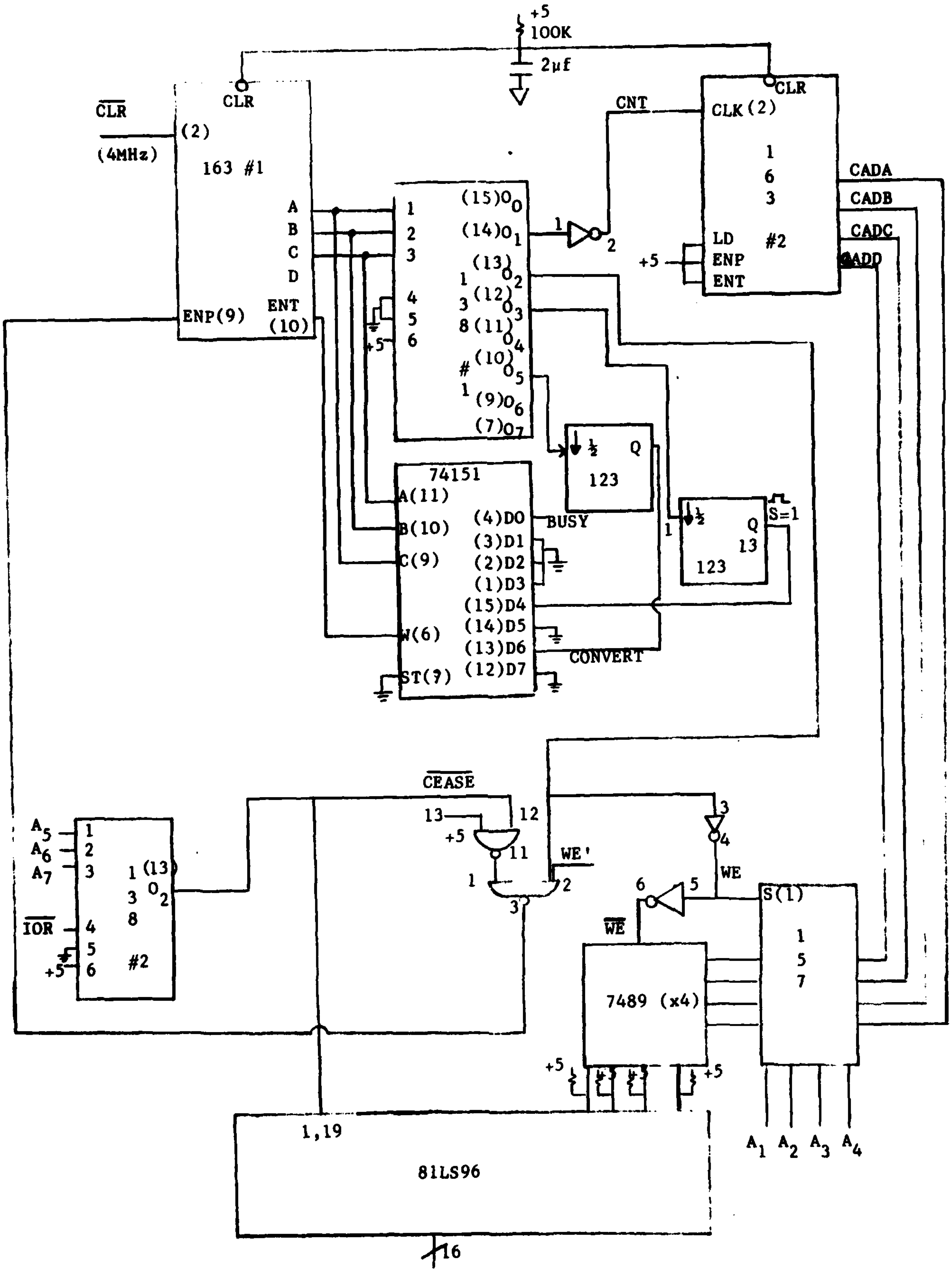


FIGURE 84. 8086 HYBRID INTERFACE BOARD

XI 28 VOLT DISCRETE I/O

A discrete I/O board was built to accept and provide 28 volt relay logic compatibility with TTL logic. The board can handle up to 32 inputs and 32 outputs. The board doesn't require a motherboard slot since it only uses +5 and gnd from the system. An external 28 volt supply must be provided through the rear panel. The overall board layout is shown in Figure 86.

<u>The Input Circuitry</u>

The input circuit is merely 32 replications of the circuit shown in Figure 85.

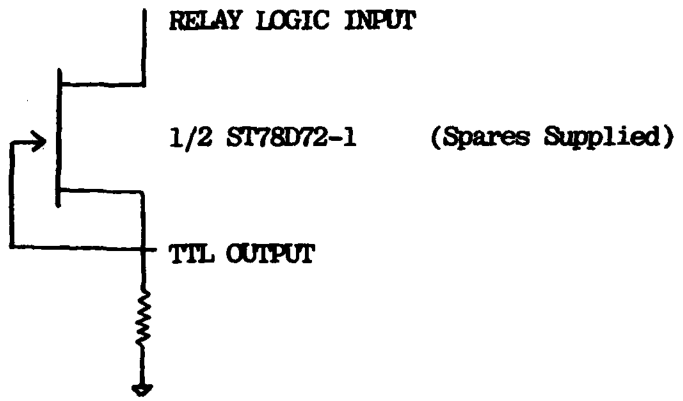


FIGURE 85. INPUT CIRCUIT

The circuit provides a constant current source over a large range of input values. The components used on the board were selected to match requirements. Testing of each input circuit and the recorded results are given in Table 11. As can be seen between 24 and 28 volts in (a relay logic "1") the circuit output provides a valid TTL "1". The output actually remains valid down to about 12 volts input. With no input the

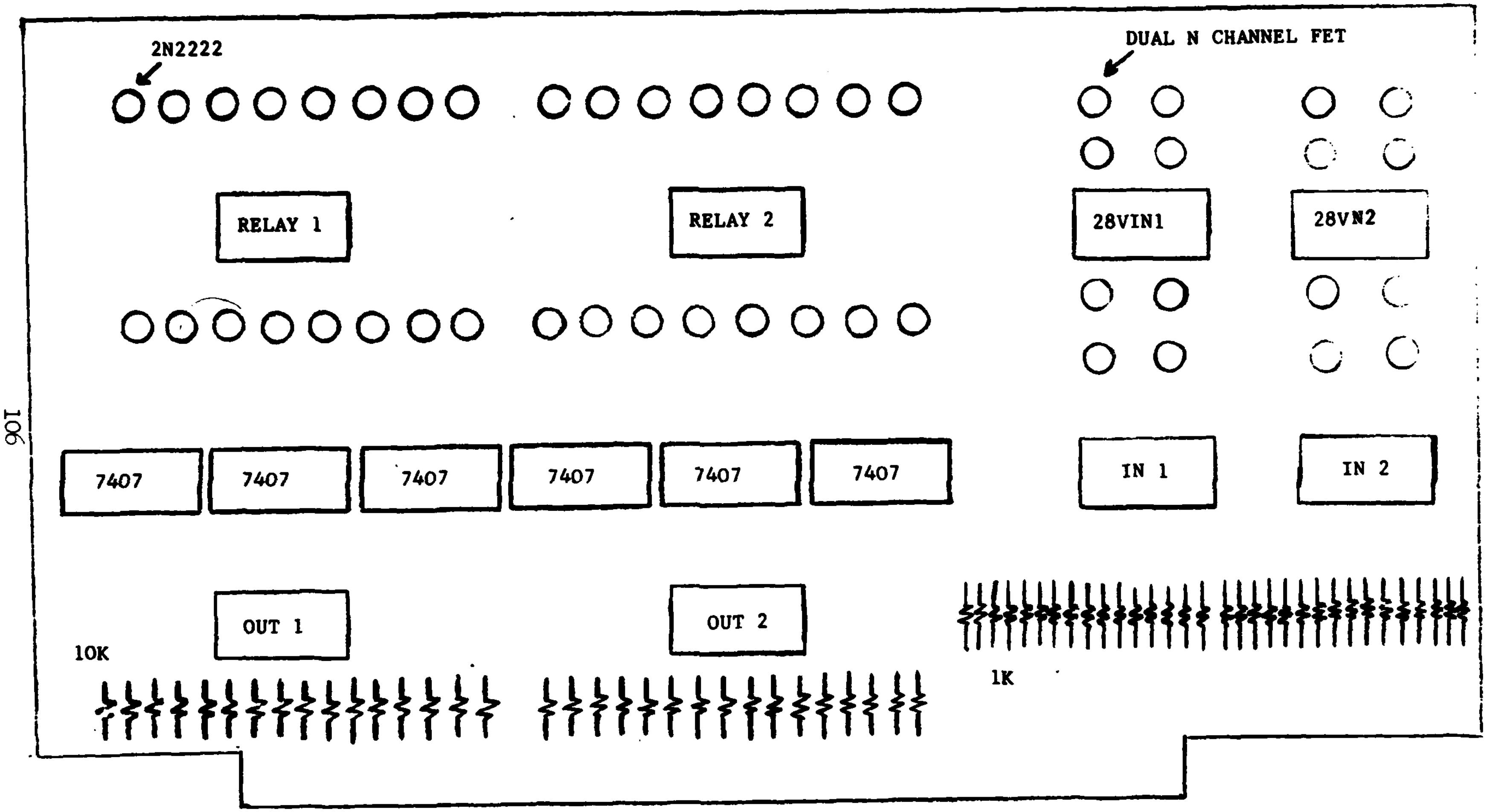


FIGURE 86
DISCRETE I/O BOARD

TABLE 11. DISCRETE I/O

OUTPUT VS INPUT VOLTAGE

PORT 0

PIN	24V	28V
1	3.0	3.0
2	3.1	3.1
3	2.8	2.8
4	3.3	3.2
5	3.2	3.2
6	4.3	4.2
7	3.2	3.2
8	4.4	4.3
9	4.7	4.7
10	2.9	2.9
11	4.7	4.6
12	3.0	3.0
13	3.0	2.9
14	2.7	2.7
15	3.0	2.9
16	2.8	2.8

PORT 1

PIN	24V	28V
1	2.7	2.7
2	3.4	3.4
3	2.6	2.7
4	3.4	3.4
5	3.7	3.7
6	2.3	2.3
7	3.8	3.8
8	2.3	2.3
9	3.0	3.0
10	3.4	3.4
11	3.0	2.9
12	3.4	3.4
13	4.8	4.8
14	2.9	2.9
15	4.9	4.9
16	3.0	3.0

OUTPUT VOLTAGE AT 50 Ma

PORT 0

PIN	VOLTAGE
1	24.9
2	24.3
3	24.5
4	25.3
5	25.0
6	25.2
7	25.1
8	25.3
9	25.2
10	25.1
11	25.2
12	24.8
13	24.7
14	24.4
15	25.0
16	25.1

PORT 1

PIN	VOLTAGE
1	25.1
2	24.6
3	24.8
4	25.0
5	25.1
6	24.9
7	24.3
8	24.9
9	24.8
10	24.6
11	25.1
12	24.5
13	25.3
14	25.0
15	24.9
16	25.0

output will be 0 volts. With a low voltage input (less than 4 volts) we are assured of a TTL logic of "0" output. From the JFET outputs the logic signals are cabled directly to the system input ports (F8, F9, FA, and FB).

Inputs are provided to this circuitry through the rear panel of the computer. D25P/S connectors are used. The pinout of the connector is shown in Table 12.

TABLE 12. D25P/S CONNECTOR PINOUT

CHANNEL	D25P/S PIN	SIXTEEN PIN CABLE
0	1	1
1	2	2
2	3	3
3	4	4
4	5	5
5	6	6
6	7	7
7	8	8
8	9	9
9	10	10
10	11	11
11	12	12
12	13	13
13	14	14
14	15	15
15	16	16

Output Circuitry

The output requirement was to be able to source 24 to 28 VDC at 50 ma. To accomplish this task the circuitry of Figure 87 was used.

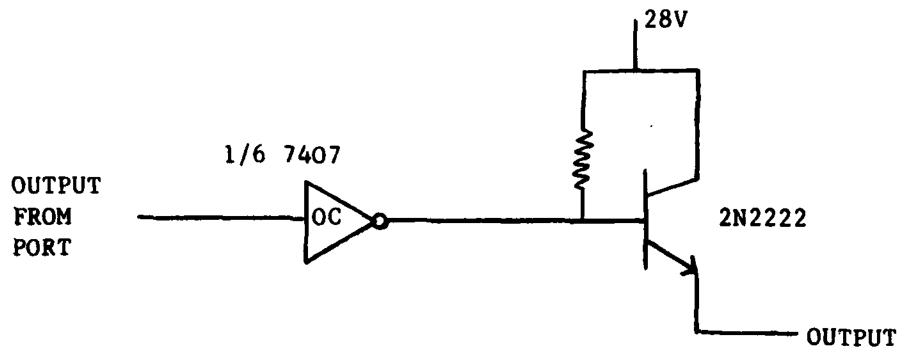


FIGURE 87. DISCRETE OUTPUT CIRCUITRY

The output of this circuit will provide up to 800 ma at which point the 2N2222 becomes a fuse. Short circuits are fatal and should be avoided at all costs. Cabling for the output discretes is identical to input cabling described in Table 12. Test results of voltage provided under 50 ma load are also given in Table 11. The inputs to the 7407's are provided from output ports F8, F9, FA, and FB.

XII. THE FLOPPY DISK CONTROLLER

The floppy disk controller based on Western Digital's 1791 circuit (16) is one of the more complex circuits in the USAFA/8086. Making the circuitry functional proved to be an extremely challenging task since we were dealing with both unknown hardware and unknown software of a reasonably complex nature. The board layout is shown in Figure 90 while the schematic of the disk controller is presented in Figure 89.

Decoding

The disk controller is an eight bit device and resides on the lower address bus. The addresses CØ, C2, C4, C6, C8, CA, CC, and CE are associated with the disk controller on its supporting circuitry. Figure 88 shows the decoding circuitry.

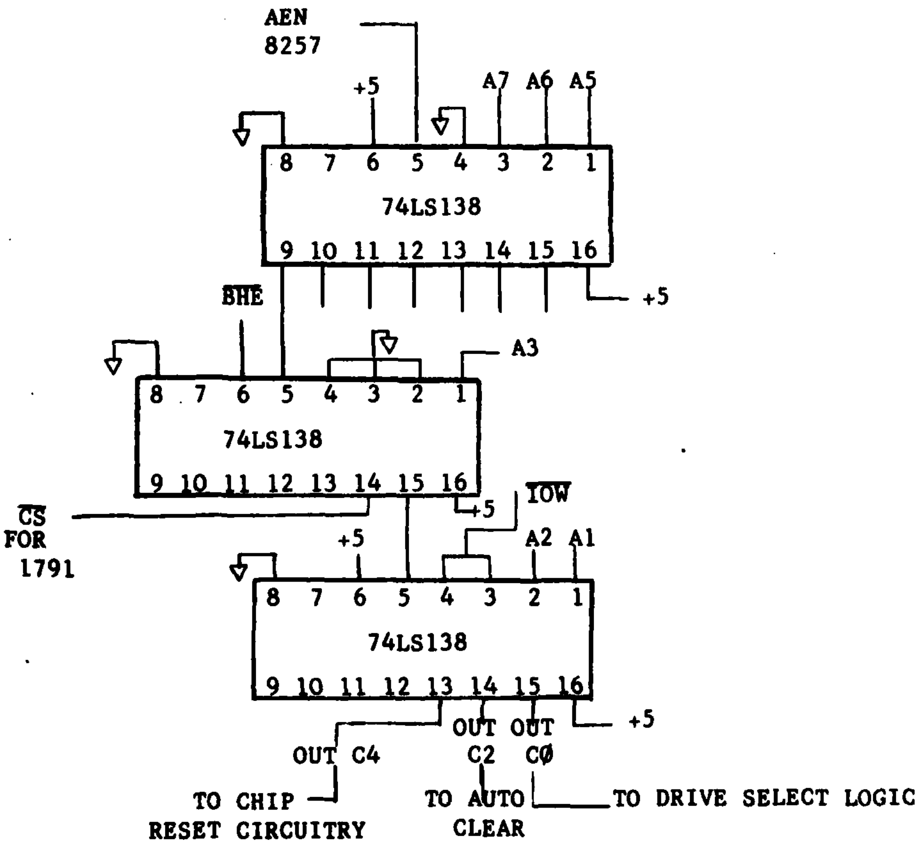


FIGURE 88. DECODING CIRCUITRY

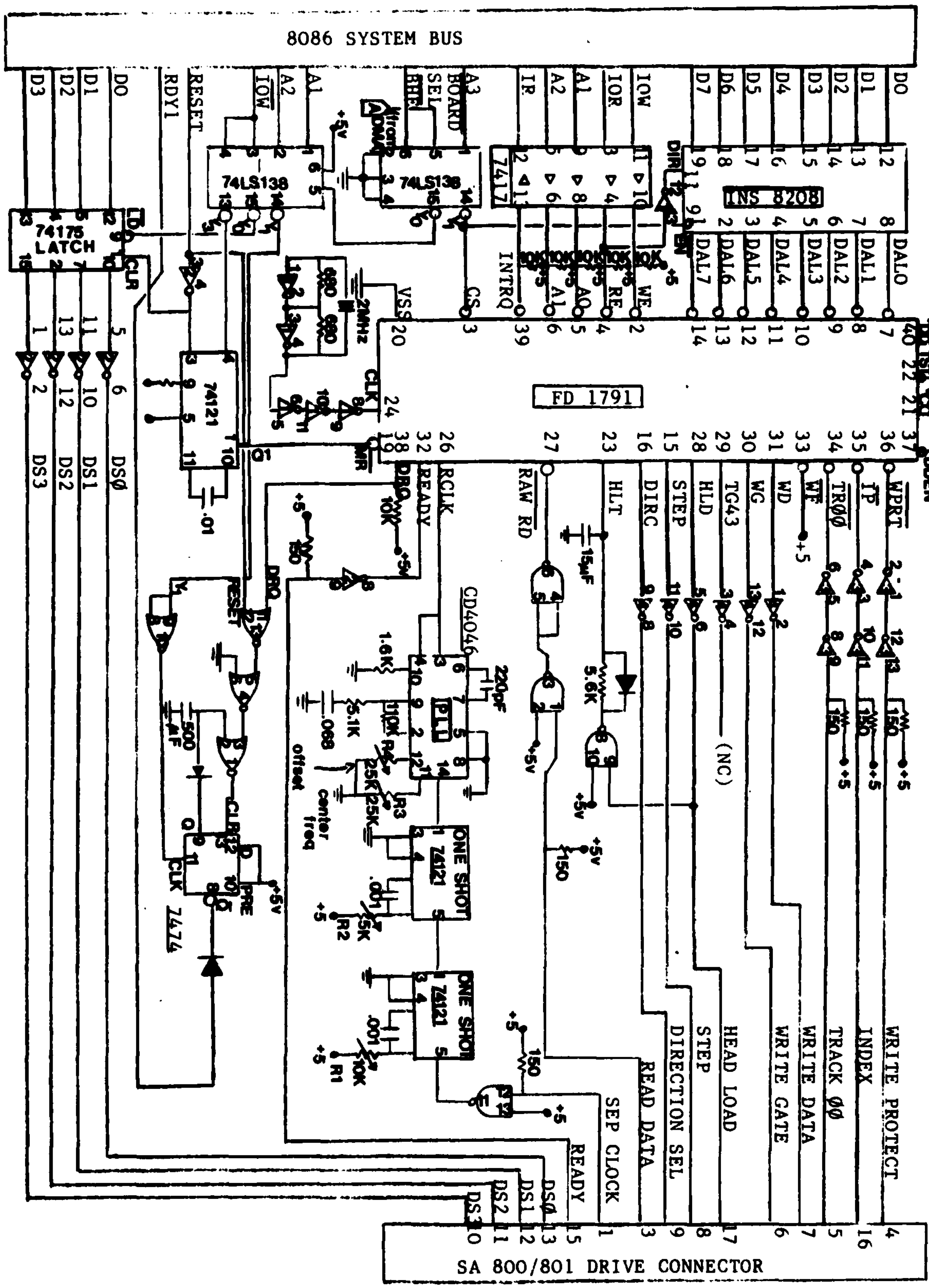


FIGURE 39. DISK CONTROLLER CIRCUITRY

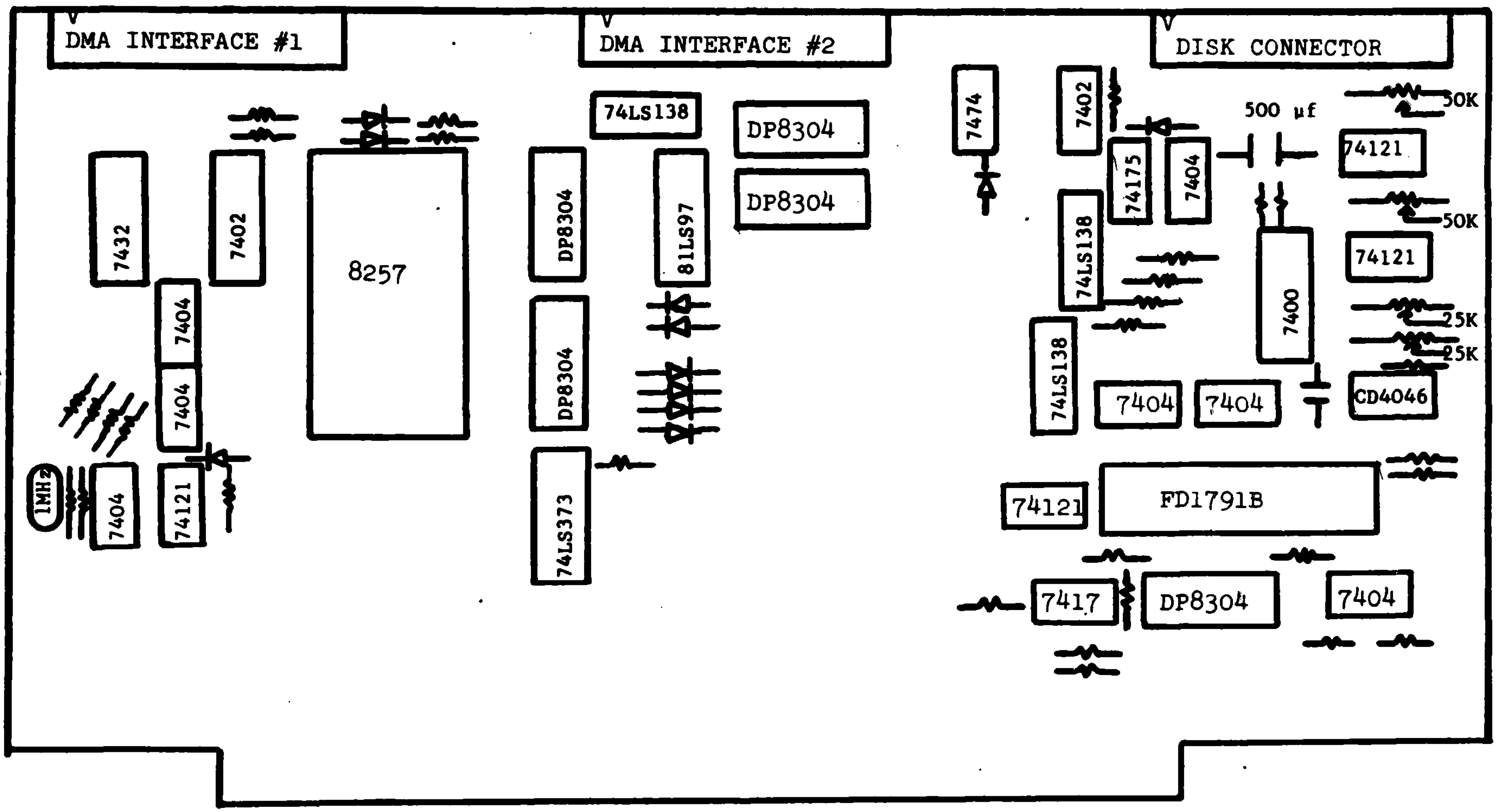


FIGURE 90
DMA/DISK CONTROLLER

Since the address lines A1 and A2 are directly connected to the 1791 the following registers are selected by the indicated address:

ADDRESS	REGISTER
C8	Status/Command
CA	Track
CC	Sector
CE	Data

Drive Select Circuitry

Standard floppy disk systems provide four device select lines into each drive. Only one is actually jumpered into the circuitry for drive selection. Thus, using a 4 bit register holding a "one hot" code any of four drives is easily selected. The circuitry of Figure 91 is used for drive selection by this controller.

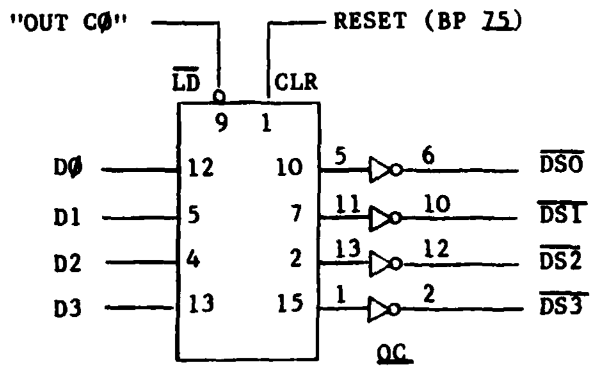


FIGURE 91. DRIVE SELECT CIRCUITRY

Table 13 shows the code corresponding to each drive.

TABLE 13. DRIVE SELECTION CODE

CODE	DRIVE
0001	Ø
0010	1
0100	2
1000	3

Note that by improper programming of this select code multiple drives can be simultaneously selected.

Reset Circuitry

The system reset (BP75) is applied to a 74121 monostable (single shot) to create the reset pulse to the 1791 Controller Chip. This reset is required to be at least 50µs in direction. A pulse of approximately 100µs is assured by the 74121 circuit. The circuitry is shown in Figure 92 .

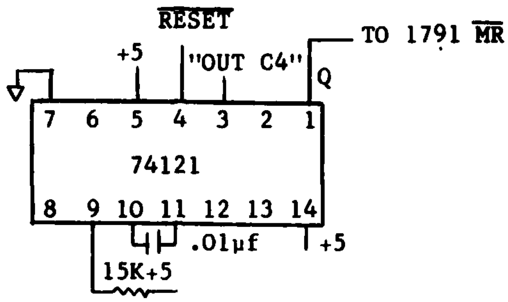


FIGURE 92. RESET CIRCUIT

The instruction "OUT C4" will also cause this circuit to trigger generating a Master Reset to the 1791 controller. The system reset is also used to clear the "auto-clearing" circuitry which was determined to not be required in the AFFDL system.

CPU Bus Buffering

The data bus is buffered by an INS8208 (identical to DP8304). Since the 1791's data bus is active low an inverting octal bidirectional tristate buffer was desirable but not available. Thus, all data transfers to and from the 1791 must be preceeded by the instruction CMA (complement data). The INTRQ line shown in Figure 89 is not connected to the system interrupts as this was not required in the implementation used. Non-inverting 7417 buffers were used to isolate the $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, A1, and A2 lines.

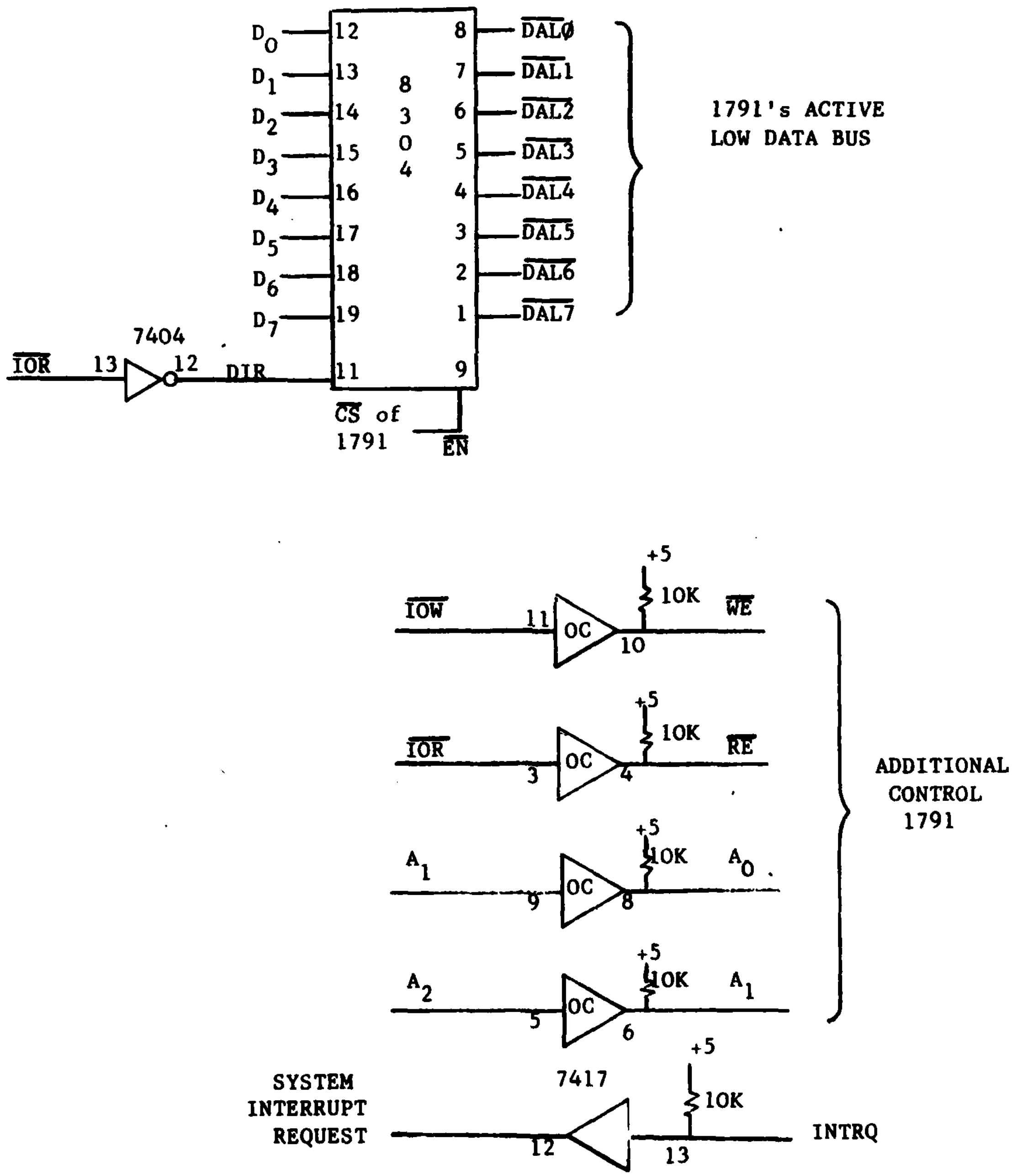


FIGURE 93. 1791 DATA/ADDRESS/CONTROL BUFFERING

The "Auto Clearing" Handshake Circuitry

Circuitry was designed for use in system debugging which is called the "Auto Clearing" handshake circuitry. The purpose of this circuitry was to artifically generate data requests (DRQ's) similar to those treated by the 1791. When the 1791 is asked to do either a sector read or sector write, it generates a number of data requests based on the number of bytes defined to be in a sector. In our case this is 128. If the CPU does not respond in a timely manner, a DRQ may be missed causing the CPU to "hang" in a loop of predetermined length. The circuit shown in Figure 94 works as follows. When either a reset or a data request was active, Pin 13 goes to logic 0. This is inverted by the second NOR gate and tied to Pin 3 of the 3rd stage NOR. So, Pin 3 is a "1" if either DRQ or RESET is active. This forces the $\overline{\text{CLR}}$ input of the 7474 D Flip Flop low causing Q to go to 0 and $\overline{Q}$ to 1. If $\overline{Q}$ is a 1 the $\overline{\text{RDY1}}$ line is forced passively high and the CPU may continue processing. Since Q is a zero, current is drained from the 500µf capacitor causing it to discharge rapidly. When the CPU executes an OUT C2 instruction the flip flop is loaded and Q=1. If Q=1 then the 500µf capacitor begins to charge. When it reaches a logic 1 voltage level the flip flop will be forced to clear. Of course the capacitor will never charge to logic 1 level if the 1791 continues to issue DRQ's on a regular basis. The sequence of expected events then is as follows.

The 1791 is directed to either read or write a sector. In response the 1791 issues a fixed number of data requests. At the beginning of the read or write loop the processor executes an OUT C2 instruction causing the handshake flip flop to make the processor not ready. If either a DRQ occurs or a reset or we "time out" the flip flop will be cleared causing the computer to execute another I/O loop. This necessarily will eventually reach the finite loop count and exit. The computer cannot hang because of an improper data transfer. Once the system was debugged, I/O Transfer from the disk was found to be reliable and the 7474 flip flop removed from the system disabling this circuitry.

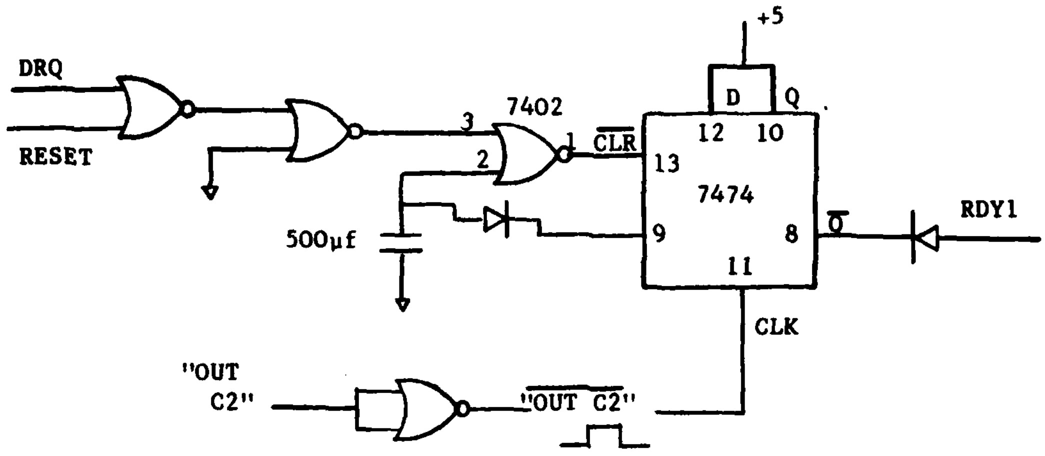


FIGURE 94. AUTO CLEARING HANDSHAKE CIRCUITRY

The 1791 Clock Circuitry

The disk controller card has provision for its own TTL 2MHz oscillator on board. However, lacking a 2MHz crystal, and having a 2MHz clock on the system bus, the PCLK signal was injected directly into the oscillator. If the CPU is run at other than 4MHz, a 2MHz crystal will have to be installed on this card if the disk system is to continue to generate properly.

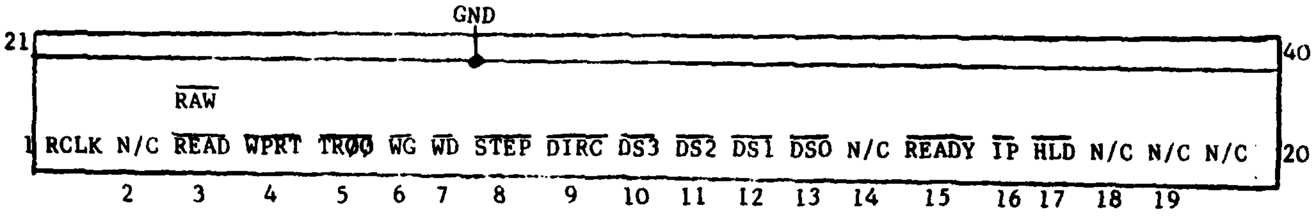
The Floppy Disk Interface

The signals required for interfacing to a floppy disk and their functions are indicated in Table 14. The signal bus is of the open collector technology type.

TABLE 14. DISK INTERFACE SIGNALS

	INPUT (I)/OUTPUT (O) OF 1791 CONTROLLER	FUNCTION
WRITE PROTECT	I	Senses whether disk is Write Protected
INDEX	I	Senses presence of the index hole
TRACK 00	I	Senses that head is over the outer-most track
WRITE DATA	O	Composite Clock/Data Signal to be written
WRITE GATE	O	Write Enable for disk electronics
HEAD LOAD	O	A command signal to load the head
STEP	O	A command to step one track
DIRECTION	O	A command to indicate the direction of the step to be taken (in or out)
READY	I	Senses a disk is present, rotating at 360 rpm with the access door closed
READ DATA	I	Composite Clock/Data input
SEPARTED CLOCK	I	Clock only information
$\overline{DS0}$, $\overline{DS1}$, $\overline{DS2}$, $\overline{DS3}$	O	Drive Selector
TG43 (TRACK GREATER THAN 43)	O	A signal to the disk system that current is to lessened on writer due to the higher density of data towards the center of the disk

As shown in Figure 89 these signals are buffered and provided to the disk system. The connector shown on the schematic is at the SA801 disks used in the USAFA/8086 system. The connector at the 1791 Controller board is as shown in Figure 95.



Pins 21 to 40 are grounded to minimize transmission effects.

FIGURE 95. DISK CONTROLLER CABLE AT DISK CONTROLLER BOARD

Head Load Timing

The signal HLD commands the selected drive to load its head. Since this is a mechanical process which is known to take about 35ms, a delay prior to confirming the Head Loaded through use of the HLT signal is necessary. Normally a monostable performs this function. However, lacking real estate for a separate monostable circuit, the circuit of Figure 96 was used. The circuit is really very simple. If HLD=1, then Pin 8 of the NAND gate is a 1. If the output of the NAND gate is a 1, then through the 5.6K resistor and the internal resistance of the gate the 20µfd capacitor charges. When it reaches 2.6 volts the 1791 will detect that the head is loaded. When the HLD command is removed the NAND gate output goes to zero and the capacitor discharges through the diode. The 20µfd value was chosen by experimentation.

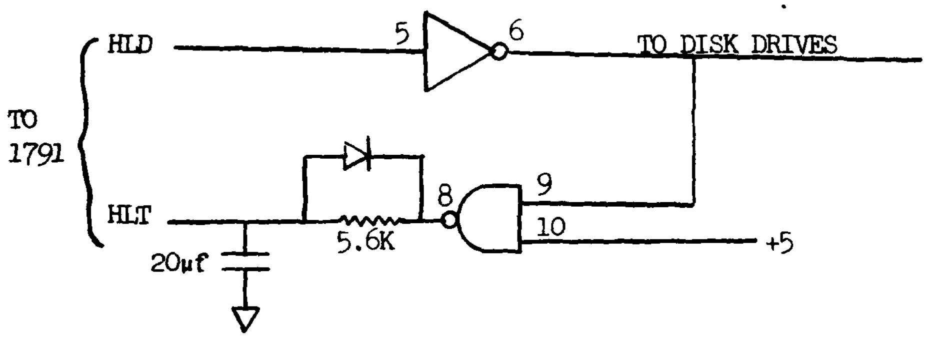


FIGURE 96. HLT TIMING CIRCUIT

Read Clock Generations

The timing between the raw read data and separated clock presented to the 1791 is extremely critical as one might expect. The manufacturers warn that delays across conditioning circuitry may invalidate the representation of separated clock and data from their disk drives. Further, the 1791 requires a continuous 50% duty cycle clock with raw read data centered in each half cycle. Figure 97 shows the proper relationship. The clock is identified as it occurs every cycle whereas a data pulse need not be present. To achieve this two monostables and a phase locked loop are used. The operation of these circuits as shown in Figure 98 is essential to understanding the read timing of the disk system.

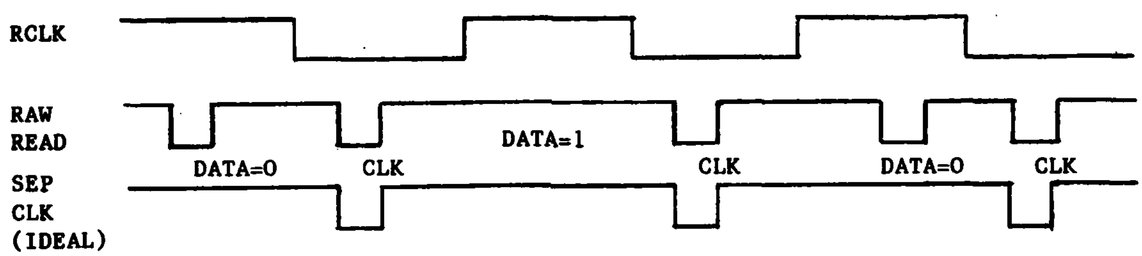


FIGURE 97. READ DATA/CLOCK TIMING

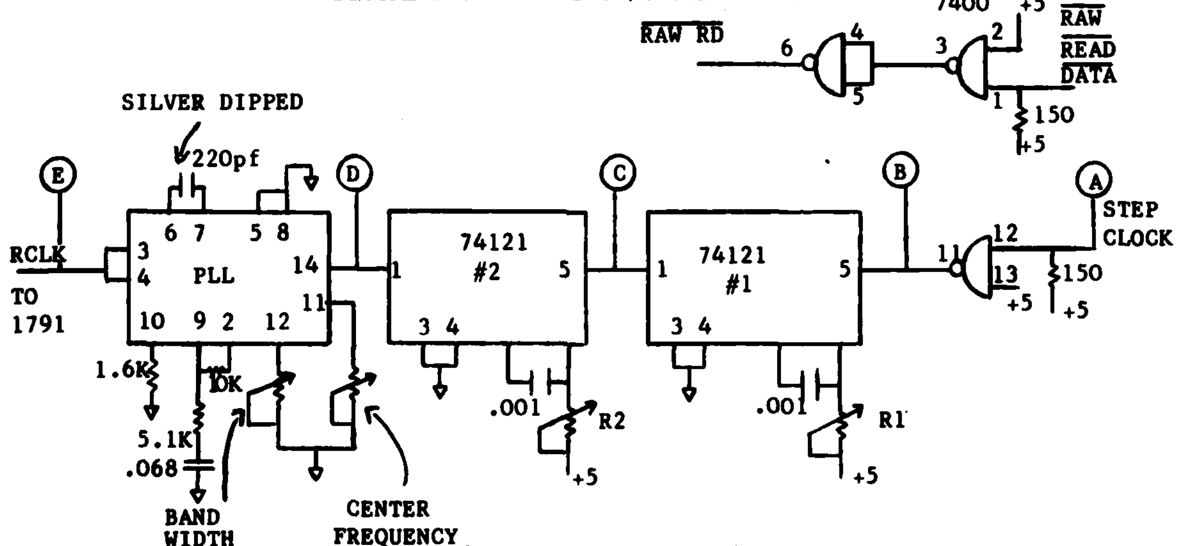


FIGURE 98. READ TIMING CIRCUITRY

The raw read data must be received from the open collector bus and then inverted again to achieve the proper polarity for application to the 1791. To understand the separated clock circuitry we will use the labels of Figure 98 and the timing diagrams of Figure 99 while discussing the calibration procedure. To calibrate the controller read circuitry the cabling to the disk drives is removed and replaced with a cable which has Pin 1 (RCLK) connected to a generator supplying a TTL compatible 250KHz square wave. The frequency should be accurate to within the capability of the equipment being used. A calibrated oscilloscope is necessary for all of the following steps. The period of the 250KHz wave is 4μs. Looking at Figure 98 we note that both 74121 circuits are identical. The monostables are rising edge triggered. Resistors R1 and R2 may be used to adjust pulse duration. The first 74121 is adjusted to produce an 875ns pulse. The second 74121 is adjusted to produce a 2.0μs pulse. The theory here is that 875ns following the rising edge of the separated clock, this pulse will be centered on the data pulse, if there is one. This is accurate to within the delay across the extra NAND gate in the raw read data circuitry plus any error introduced by the disk electronics. With the generator off the phase locked loop is adjusted for 255KHz center frequency with a bandwidth of about 100KHz. Unfortunately, R3 and R4 are interactive. However, nominal values of all protentiometers are given in Table 15. When this is complete the disk cable is reinstalled.

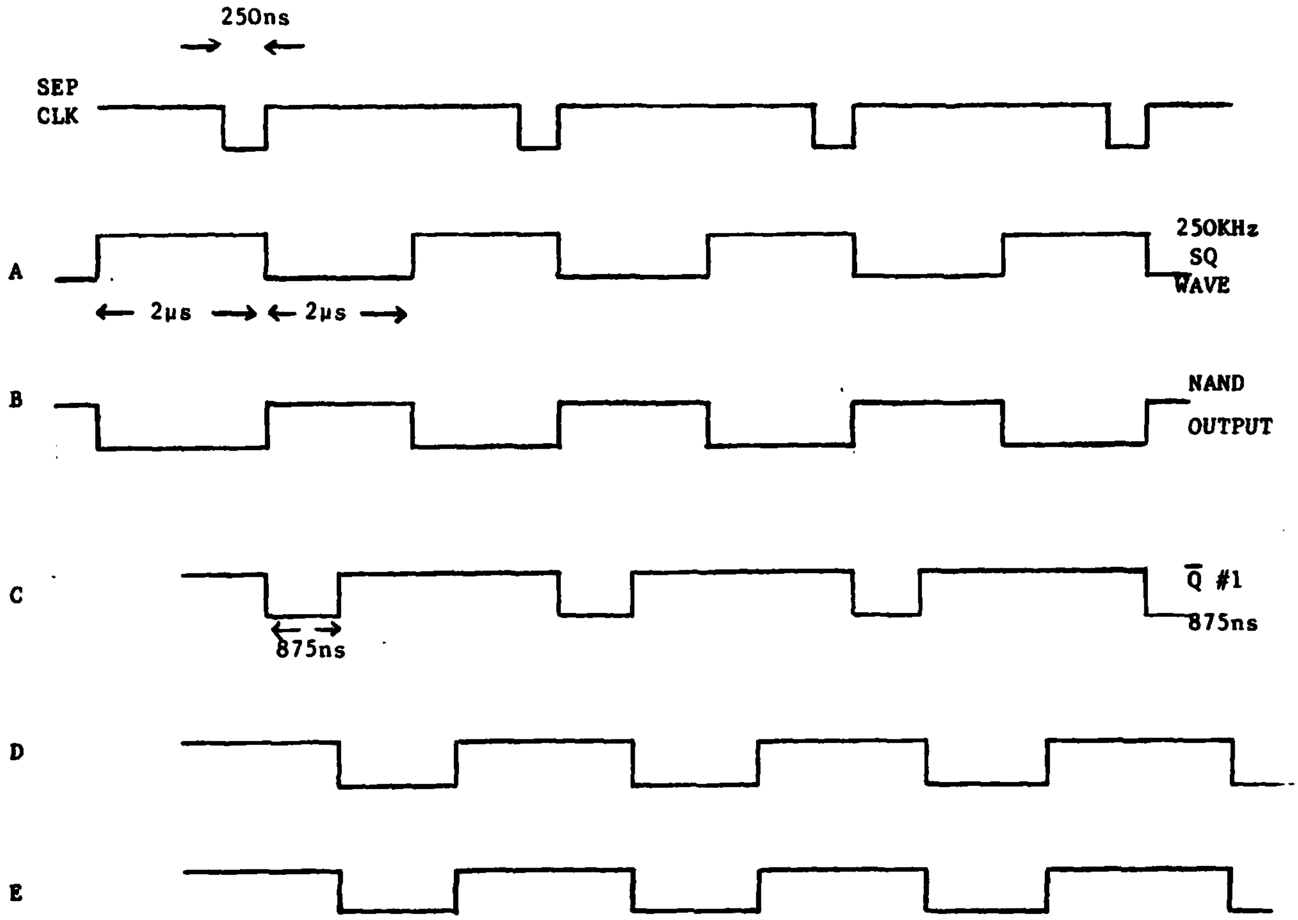


FIGURE 99. CALIBRATION TIMING OF THE DISK CONTROLLER

TABLE 15. DISK CONTROLLER POTENTIOMETER SETTINGS

RESISTOR	NOMINAL VALUE
R1	1.1K
R2	3.94K
R3	5.60K
R4	15.36K

The phase locked loop <u>is</u> voltage sensitive to charges in V_{CC}. All calibration should be performed with the system supply voltage between 4.95 and 5.05 volts. The silver dipped capacitor is essential for power on stability, i.e., minimization of change with change in operating temperature. A physical drawing of the SA-801 Disk Drive is given in Figure 100.

This concludes the discussion of the disk controller hardware. Excellent references to floppy disk operations are provided by Shugart Associates, (17), (18), (19), and (20). These should be consulted for a more thorough understanding of floppy disk operations, formats, and maintenance.

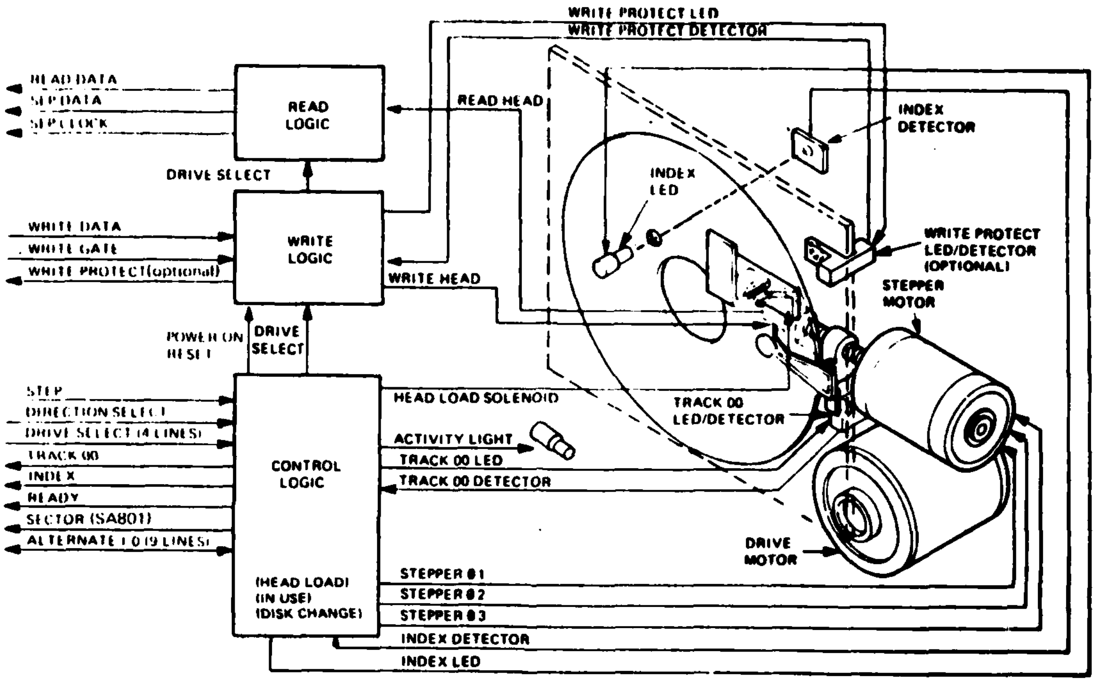


FIGURE 100. SHUGART 801 DISK DRIVE

XIII. DIRECT MEMORY ACCESS CONTROLLER

The direct memory access controller (DMA) for the USAFA/8086 was designed around the Intel 8257 (12:12-98). The DMA controller resides on the same board as the floppy disk controller. Figure 90 shows the parts layout for the board while Figure 102 shows the schematic for the DMA controller.

Decoding

The decoding circuitry consists of two parts. The first is partially shared in common with the floppy disk controller. Figure 101 shows the 8257 chip select circuitry.

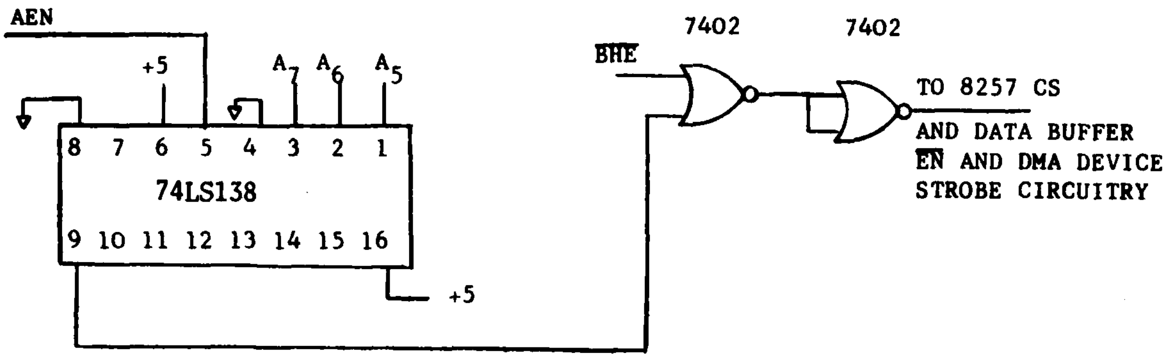


FIGURE 101. 8257 CHIP SELECT CIRCUITRY

The circuit selects on all memory or I/O addresses having $A_7A_6A_5$ = 110 and $\overline{BHE}$. In particular all odd addresses in the I/O space "CX" and "DX" are selected. The AEN signal is asserted active high by the DMA controller while it is using the data, address, and control busses. This interlock is redundant and inhibits the 8257 from selecting itself during DMA operations. The second part of the decoder circuitry is shown in Figure 103. This part of the circuitry is actually not directly related to the DMA controller but rather merely uses discrete gates, a diode resistor logic AND gate and the board select signal to cause a strobe called LD to be issued to the DMA device connected via the DMA controller interface cables.

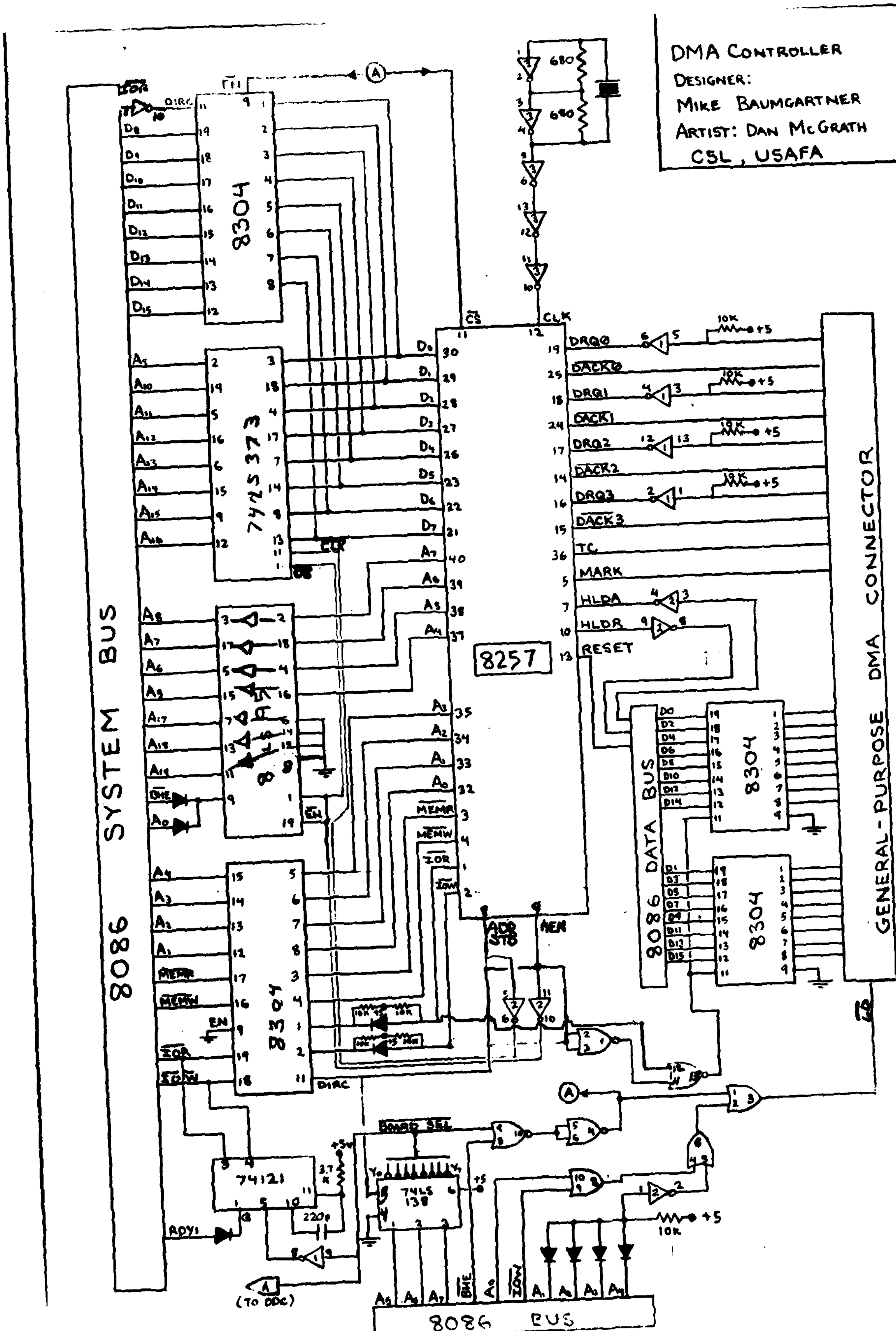


FIGURE 102. DMA CONTROLLER SCHEMATIC

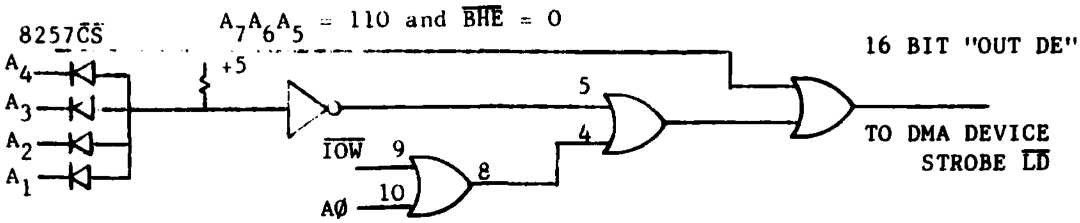


FIGURE 103. DMA DEVICE STROBE

Data Bus Buffering

The 8086 high order data bus is connected to the 8257 data lines to allow programming of the LSI device as well as the reading of its status. Since this 8257 data bus is actually a multiplexed address/data bus, the DP8304 used for buffering cannot be continuously enabled but, rather, must be enabled only while the 8257 is selected. The direction control on the buffer is connected to IOR and keeps the buffer pointed toward the 8257 except when an IOR is actually requested. This prevents the obvious problem of bus contention when the 8257 is inadvertantly selected during memory addressing. This circuit is shown in Figure 104.

The 8086 data bus (all 16 bits) must also be available during the DMA operations. Two DP8304's provide buffers which are only directed onto the data bus during DMA transfers when AEN=1 and $\overline{IOR}$=0. The buffers responsed only when $\overline{IOR}$=0 due to DMA activity. Figure 105 shows the circuitry.

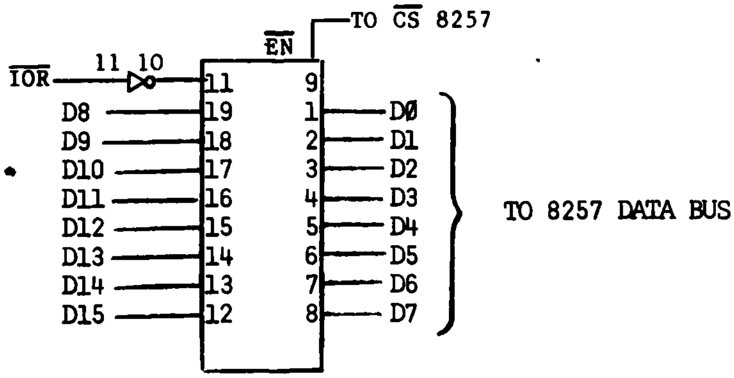


FIGURE 104. DATA BUS BUFFERING FOR DMA PROGRAMMING

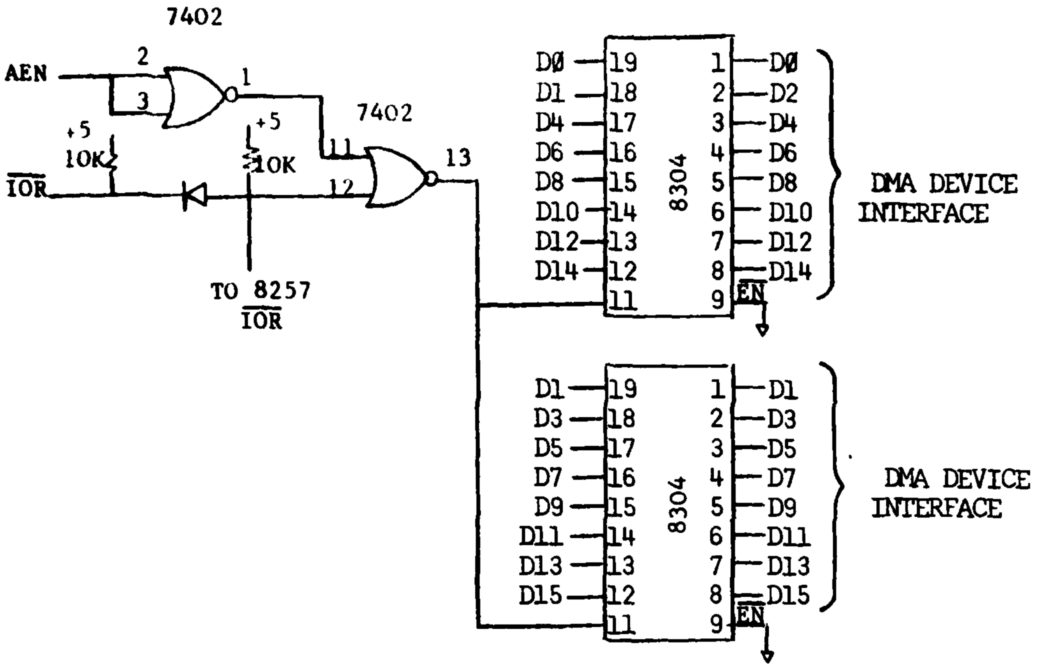


FIGURE 105. DATA BUS BUFFERING FOR DMA ACTIVITY (16 BIT)

Address/Control Bus Buffering

The 8257 receives address information directly on Pins 32, 33, 34, and 35 for use in programming its many internal registers. The 8257 also provides information on these lines while it is bus master and accessing memory. Therefore, the need for a bidirectional buffer on address lines A_1, A_2, A_3, and A_4 exists. The same argument holds for the $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ signals since they must be able to be asserted by the 8257. The $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ lines, however, are special. The 8086 bus communicates with the 8257 over these lines. However, there are no DMA I/O devices on the 8086 bus and so it has no need to drive IOR and IOW. To use the remaining two buffers the diode resister circuitry shown is used. This doesn't allow the 8257 IOR/IOW commands to enter the 8086 system bus.

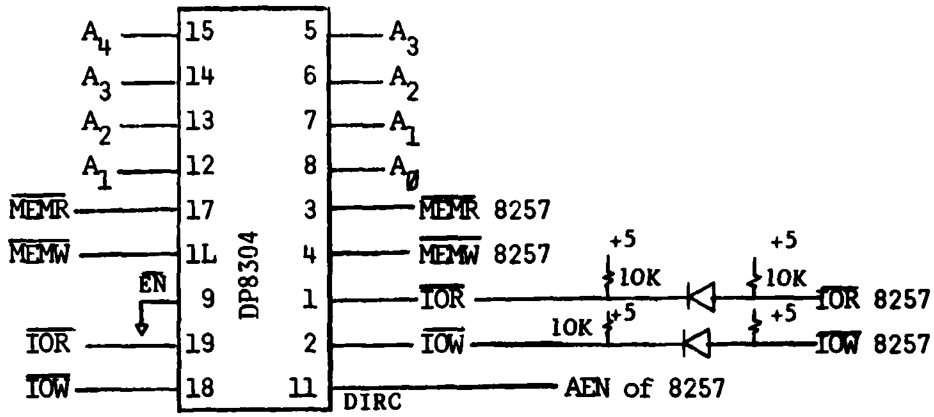


FIGURE 106. BIDIRECTIONAL DMA ADDRESS CONTROL BUFFERING

The upper eight bits of the DMA address are multiplexed on the 8257 data bus and must be demultiplexed for use in the DMA cycle. The 8257 provides and ADSTB signal (address strobe) to assist in this process. Figure 107 shows the required address latch.

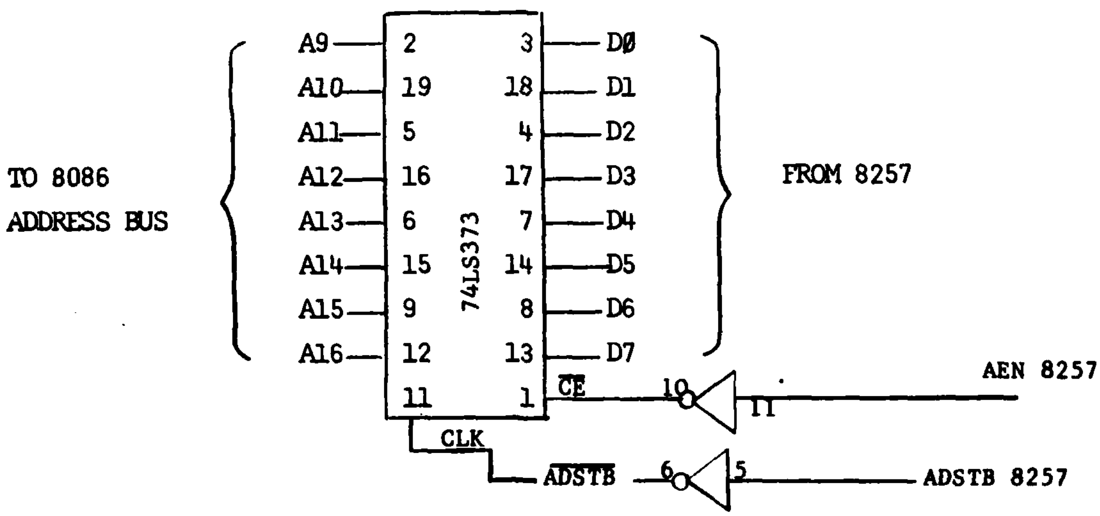


FIGURE 107. ADDRESS DIMULTIPLEXING FOR THE 8257

There are 9 additional address and control lines which are handled in a unidirectional manner using the 81LS95. The circuitry is shown in Figure 108. The control lines AØ and $\overline{BHE}$ are both pulled low through the indicated diode arrangement so that the 8086 system understands all DMA operations are to be of a sixteen bit nature.

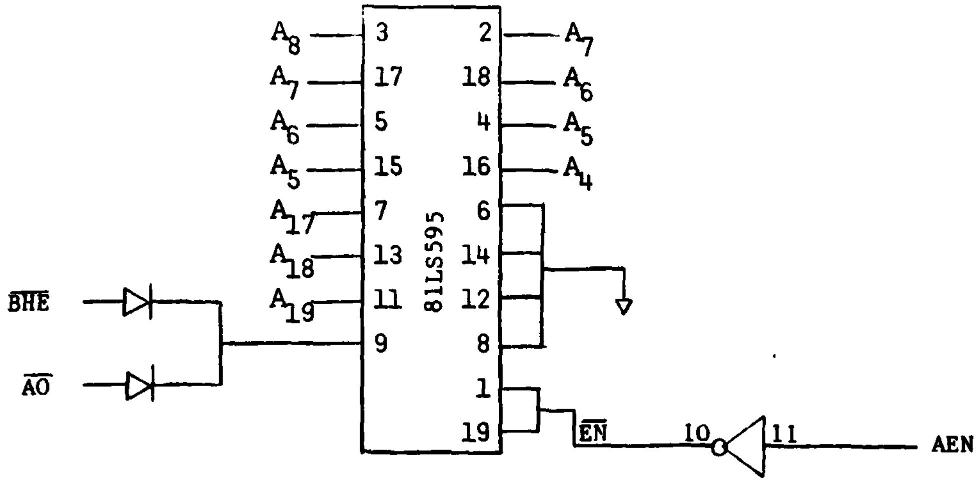


FIGURE 108. UNIDIRECTIONAL ADDRESS CONTROL BUFFERING

As can be seen, address lines A_{17}, A_{18}, A_{19} are handwired to 0 for all DMA operations.

Read/Write Delay Circuitry

The 8257, like many Intel LSI circuits, cannot respond at a speed acceptable to a 4MHz processor. This necessitates the use of the system ready line to slow the processor while it communicates with the 8257.

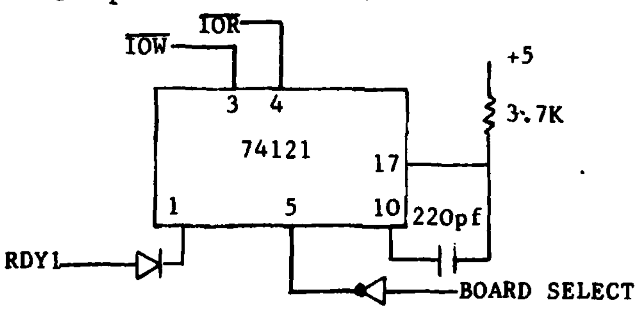


FIGURE 109. 8257 ACCESS DELAY CIRCUIT

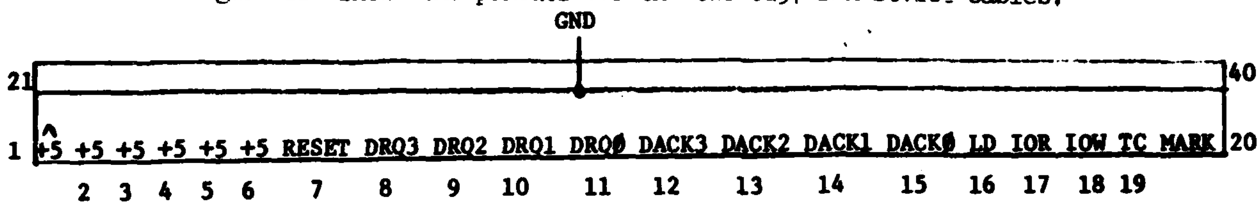
The RC combination provides a not ready signal of about 550ns duration. This delay actually occurs on all I/O reads and writes within the range of the board (C0-DF).

The 8257 Clock

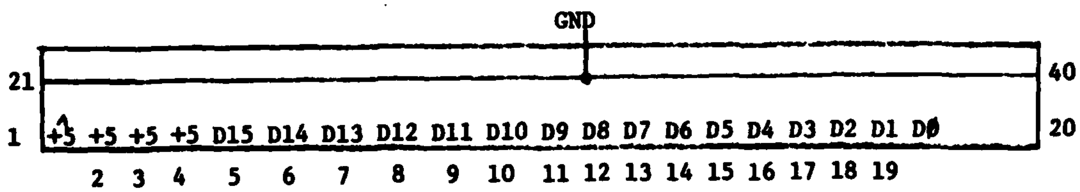
The 8257 must be provided a clock between 3MHz and 250KHz. Speed of transfers is directly related to this clock. The clock applied to the AFFDL processor is the 2MHz system PCLK although circuitry would support an independent crystal oscillator.

DMA Device Interface

Figure 110 shows the pinouts for the two 8257 DMA Device Cables.



CONNECTOR #1



CONNECTOR #2

On both connectors pins 21 through 40 are grounded to minimize transmission effects.

FIGURE 110. DMA DEVICE CABLES

The theory of operation of the 8257 is described thoroughly in Reference 12.

XIV. THE SYSTEM PERIPHERALS

The system peripherals consist of:

a. a RCA VIP601 ASCII Keyboard

b. a CRT-1000 Display Controller

c. a 12" Ledex Video Monitor

d. a Centronix Microprinter P-1

Interconnecting the VIP601

The VIP601 as delivered by the manufacturer has two minor difficulties for application in the USAFA/8086 system. First, the active high strobe pulse provided is 15ms. We prefer to use a 50μs pulse. To allow this pulse width all that is necessary is that capacitor C6 be changed from .047μf to 180pf. Secondly, the connector supplied on the printed circuit board is non-standard and does not match any other in the system. The connector was removed and one end of a sixteen pin cable directly connected to the printed circuit. Minor modification to the case was necessary to allow proper strain relief. The pinout used for the cable is shown in Figure 111 below. The cable is connected to input ports $F\emptyset_H$ and $F1_H$.

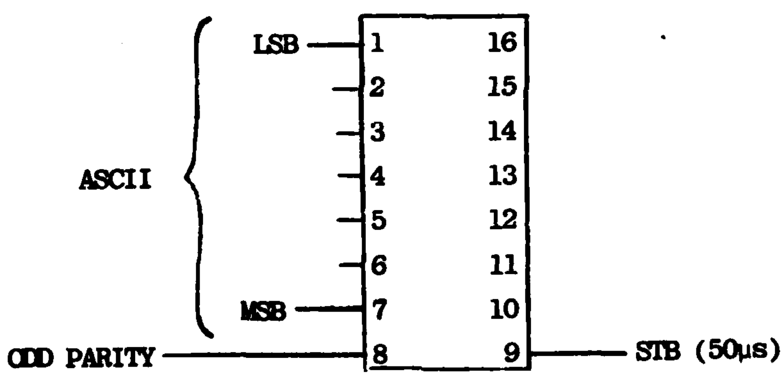


FIGURE 111. VIP601 CABLE PINOUT

The keyboard is strapped to allow both upper and lower case generation. The documentation provided by the manufacturer is generally weak (21).
Power connections are made to the keyboard over a system standard 10 pin power connector although only 5V and GND are required.

The CRT-1000 Video Interface

This video interface was purchased rather than built due to the complexity of mixing digital and video information on the same PC board. The low cost of about $125 made local manufacture not feasible. The board is very simple from an interface point of view requiring only that 7 bit ASCII be transmitted along with an active high strobe. The connecting cable is described in Figure 112. The cable is connected to output port $F\emptyset_H$. Port $F1_H$ is not populated.

SIGNAL	CRT-1000 PIN	CABLE PIN
D0	1	1
D1	2	2
D2	3	3
D3	4	4
D4	5	5
D5	6	6
D6	7	7
STR	8	8

FIGURE 112. DATA CONNECTION TO THE CRT-1000

Power is supplied directly from the star connection point on the system motherboard. The video output is run over coaxial cable to the rear panel from which the video signal is carried directly to the Video Monitor. The

CRT-1000 documentation is reasonably complete showing circuitry as well as providing thorough software timing guidance. (22)

Ledex Video Monitor

The only outstanding characteristics of the Ledex Video Monitor are that it accepts direct composite video, has 12MHz bandwidth, and is reasonably priced. Coarse adjustments for the vertical and horizontal oscillators are internal and require cabinet removal. These, once adjusted, have proven stable and no problem. (23)

The Centronics Microprinter P1

The Centronics printer at the time of purchase (DAR required) was among the only inexpensive hardcopy devices with commonly available paper, multiple pitch capability, and direct parallel interface. Since then many other competitors have entered the market in the same price range. The printer has proven reliable during system testing. The manufacturer provided quality documentation (24) as well as electronic schematics which have not yet been necessary. The copy, although of unusual size, has proven to be of excellent readability, especially when copied. A sample output created during testing is shown in Figure 113.

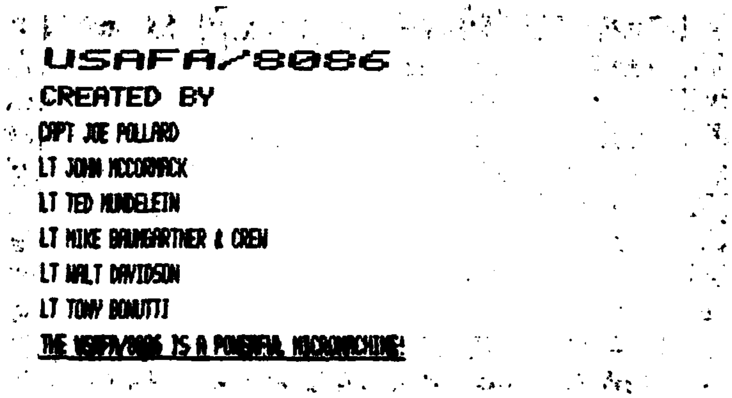

USAFA/8086
CREATED BY
CAPT JOE POLLARD
LT JOHN MCCORMACK
LT TED MUNDELEIN
LT MIKE BAUMGARTNER & CREW
LT WALT DAVIDSON
LT TONY BONUTTI
THE USAFA/8086 IS A POWERFUL MICROMACHINE!

FIGURE 113. CENTRONICS MICROPRINTER OUTPUT

Cabling to the microprinter is through a mating 36 pin connector; over a 16 pin cable to a 16 pin connector. The 16 pin connector then splits input and output signals to two sixteen pin cables which are connected to input and output ports FC_H. Figure 114 shows the cabling.

SIGNAL	MICRO PRINTER CONNECTOR	PIN #S INTERMEDIATE CONNECTOR	INPUT CABLE	OUTPUT CABLE
Data Strobe	1	8	x	8
Data Bit 1	2	1	x	1
Data Bit 2	3	2	x	2
Data Bit 3	4	3	x	3
Data Bit 4	5	4	x	4
Data Bit 5	6	5	x	5
Data Bit 6	7	6	x	6
Data Bit 7	8	7	x	7
$\overline{\text{Acknowledge}}$	10	16	1	x
Busy	11	15	2	x
Paper Out	12	14	3	x

FIGURE 114. MICROPRINTER CABLING

A separate ground is connected to the system star ground point at the motherboard. The following programming guidelines are provided for using the microprinter:

a. A carriage return $ØD_H$ automatically provides a line feed.

b. Underscore and font must be initialized prior to printing.

c. Output strobe must be strobed and busy bit checked prior to next character transmission.

CONCLUSION AND RECOMMENDATIONS

The USAFA/8086 has been a significant and exciting challenge to the faculty and students of the Department of Electrical Engineering at the U.S. Air Force Academy. The total research cost of this project was approximately $23,500 from which two working systems and some spare parts were obtained. Approximately 1.5 manyears of faculty effort were expended by Captain Pollard. In all, eleven Electrical Engineering and Engineering Science majors were directly exposed to the project through nine projects in El Engr 464 (Senior Design) and five projects in El Engr 499 (Independent Studies in Electrical Engineering). Regardless of the fate of the two existing systems, the atmosphere of research and inquisitive investigation provided in the Computer Systems Laboratory through this project, in my opinion, more than recovered the cost of the systems to the U.S. Air Force Academy.

I recommend the faculty of the Department of Electrical Engineering become more involved in research projects of this type where meaningful and difficult problems are investigated. I recommend the concepts and technology of the USAFA/8086 to those desiring to employ a 16-bit microprocessor based system in either research or education.

REFERENCES

1. Redifon Reference, June

2. IN234-78-2 Instructions for Vector 8803 Motherboard for S100 Bus Microcomputer, Vector Electronic Company, Inc., Sylmar, California

3. Q-Series Open Frame Power Supplies Instruction Manual, Deltron, Inc., North Wales, Pennsylvania

4. Power/Mate Power Supplies Condensed Catalog, Power Mate Corporation, Hackensack, NJ

5. Linear Integrated Circuits Data Book, Fairchild Semiconductor, Mountain View, CA, 1976

6. MCS86 Product Description, Intel Corporation, Santa Clara, CA, February, 1979

7. Signetics Digital Linear MOS Data Book, Signetics Corporation, Sunnyvale, CA, 1974

8. The TTL Data Book for Design Engineers, 2nd Edition, Texas Instruments, Inc., Dallas, TX, 1976

9. DP8304 8 Bit Bidirectional Transceivers, National Semiconductor, Santa Clara, CA, 1977

10. Component Data Catalog, Intel Corporation, Santa Clara, CA, 1979

11. MK4118 (P/N) Series Data Sheet, Mostek, Carrollton, TX, 1978

12. National Semiconductor TTL Data Book, National Semiconductor, 1976, Santa Clara, CA

13. AM9511 Data Sheet, Advanced Micro Devices Inc., Sunnyvale, CA, 1978

14. AD565 Data Sheet (C485-8-9/78), Analog Devices, Norwood, MA, 1975

15. AD171J Data Sheet (C166C-10-2/75), Analog Devices, Norwood, MA, 1975

16. FD1791A/B Data Sheet, Western Digital Corporation, Newport Beach, CA

17. IBM Compatibility Reference Manual, Diskette Storage Drive, Shugart Associates, 1977, Sunnyvale, CA

18. SA800/801 Diskette Storage Drive, OEM Manual, Shugart Associates, 1977, Sunnyvale, CA

19. System Implementation, SA400/450 Minifloppy Diskette Storage Drives With an 8080A/FD1771 Single Density System Application Bulletin, 1977, Shugart Associates, Sunnyvale, CA

20. SA800/801 Diskette Storage Drive, Maintenance Manual, Shugart Associates, 1977, Sunnyvale, CA

21. VP601 ASCII Keyboard Instruction Manual, RCA Cosmac VIP Marketing, Lancaster, PA

22. CRT-1000 Video Interface, Nucleonic Products Company, Canoga Park, CA, April 1978

23. Leedex All Transistor Portable Monitor (Model: Video 100), Leedex Corporation, Elk Grove Village, IL

24. Microprinter-P1 Operator's Manual, Centronics, Hudson, NH, Jan 1978

APPENDIX A

COST ANALYSIS ESTIMATE

This appendix estimates on a board by board basis the cost of the parts and materials used in construction of the USAFA/8086 designed for AFFDL.

WPAFB 8086 COST ESTIMATE

Front Panel/Single Step	$ 116.04
Rear Panel	50.18
Card Cage/Motherboard	213.19
Video Display/Microprinter	775.18
Disk Sub System	1514.81
Keyboard	66.88
Hybrid Subsystem	983.35
System Power Supply	168.33
CPU Board	426.22
APU Board	278.00
PROM Board	775.76
RAM Board (2)	1007.52
Parallel Input Board	83.77
Parallel Output Board	187.51
Discrete I/O Board	65.20
Disk Controller/DMA Board	182.21
Front Panel Interface Board	No Charge
Hybrid Interface Board	130.85
A/D Controller Board	54.20
A/D Board	No Charge
D/A Board (8) @ $262.54	2100.32
Serial I/O Interface	15.61
TOTAL	$9195.13

	QTY	PRICE	TOTAL
FRONT PANEL/SINGLE STEP			
DPST Switches	18	$ 2.00	$ 36.00
PB Switches	3	2.00	6.00
LED w/holder	20	.66	13.20
16 Pin ww Sockets	9	.84	7.56
14 Pin ww Sockets	2	.37	.74
24 Pin ww Sockets	5	.91	4.55
40 Pin Edge Connect/Mate	1	10.30	10.30
FND 500	9	.99	9.91
9368	9	2.35	21.15
7400	1	1.33	1.33
7474	1	1.37	1.37
Banana Socket	4	.15	.60
Perf Board	1	3.33	3.33
SUBTOTAL			$116.04
REAR PANEL	1	$ 6.95	$ 6.95
Power Strip	1	19.95	19.95
Fuse Holder	1	1.00	1.00
Fan	1	15.51	15.51
Power Connector Female	3	1.60	4.80
Power Connector Male	1	.87	.87
TTY Connector	1	1.10	1.10
SUBTOTAL			$ 50.18

	QTY	PRICE	TOTAL
Vector VP-1 Card Cage	1	$130.00	$130.00
11 Slot S-100 Motherboard	1	29.95	29.95
330Ω Resistors 1/2 watt	100	.03	3.00
2N2955	1	1.37	1.37
2N2907	1	.18	.18
2N2222	1	.18	.18
2N3055	1	1.10	1.10
SUBTOTAL			$165.78
Misc Resistors	8	$ .03	$ .24
Potentiometer (1K)	1	.86	.86
Capacitors (35μfd)	5	.45	2.20
Op Amp (LM4250)	1	-	-
S-100 Edge Connector	11	3.95	43.45
LED	1	.66	.66
SUBTOTAL			$ 47.41
<u>VIDEO DISPLAY</u>			
Video Terminal	1	$129.95	$129.95
Video Interface Board (CRT-1000)	1	119.95	119.95
16 Pin ww Socket	1	.84	.84
Coax Connector	1	4.12	4.12
Coax Cable/w Connectors	1	-	-
Microprinter	1	495.00	495.00
Connector	1	-	-

	QTY	PRICE	TOTAL
VIDEO DISPLAY (CONT)			
16 Pin ww Socket	3	$ .84	$ 2.52
Paper (Rolls)	3	7.50	22.50
Perf Board	1	-	-
Banana Connectors	2	.15	.30
SUBTOTAL			$775.18
DISK SUBSYSTEM			
Power Supply (CP 206)	1	$ 91.00	$ 91.00
SA 801R	2	625.00	1350.00
Connectors 40 pin	2	6.05	12.10
Jones Strip	1	1.40	1.40
Fan	1	15.51	15.51
Switch	1	2.00	2.00
LED	1	.66	.66
Power Cable	1	2.00	2.00
Floppy Diskettes	6	6.69	40.14
SUBTOTAL			$1514.81
Keyboard	1	$ 60.00	$ 60.00
74121	1	1.50	1.50
Perf Board	1	3.33	3.33
Connector	1	-	-
14 Pin ww Socket	1	.37	.37
16 Pin ww Socket	2	.84	1.68
SUBTOTAL			$ 66.88

	QTY	PRICE	TOTAL
HYBRID SUBSYSTEM			
100v Power Supplies	2	$339.00	$678.00
40 pin Connectors	2	6.05	12.10
40 pin Card Cage	1	28.82	28.82
40 pin Edge Proto Card	1	7.77	7.77
330Ω Resistors	10	.03	.30
40 pin Edge Connectors	10	5.46	54.60
Coaxial Connectors	48	4.12	197.76
Backplane	2	2.00	4.00
SUBTOTAL			$983.35
System Power Supply	1	$166.73	$166.73
Connector Female	1	1.60	1.60
SUBTOTAL			$168.33

CPU BOARD	QTY	PRICE	TOTAL
MCS-86 Kit (Includes 8086, 8288, 8284, 8282(2), 8286(2), 8259)	1	$360.00	$360.00
8282	1	8.00	8.00
12 MHz XTAL	1	7.92	7.92
7400	3	1.33	3.99
7474	2	1.37	2.74
74174	1	.67	.67
7406	1	1.78	1.78
7408	1	.31	.31
7404	1	1.01	1.01
8160	1	2.00	2.00
74LS138	1	.72	.72
81LS95	1	1.44	1.44
DPST Switch	1	2.00	2.00
7403	1	1.33	1.33
16 Pin Sockets ST	3	.51	1.53
14 Pin Sockets ST	9	.21	1.89
20 Pin Sockets ST	7	.32	2.24
40 Pin Socket ST	1	1.39	1.39
28 Pin Socket ST	1	1.10	1.10
18 Pin Socket ST	1	.50	.50
Capacitors (Min)	18	.37	6.66
PC Board	1	2.00	2.00
Artwork	-	10.00	10.00
Manufacture	-	5.00	5.00
TOTAL			$426.22

APU BOARD	QTY	PRICE	TOTAL
74163	2	$ .57	$ 1.14
74154	2	2.00	4.00
7404	2	1.01	2.02
7432	3	.26	.81
7476	2	1.87	3.74
7408	4	.31	1.24
81LS97	1	1.44	1.44
7402	1	1.25	1.25
7406	1	1.78	1.78
8282	2	8.00	16.00
74LS138	1	.72	.72
7427	1	1.40	1.40
DP8304	2	1.50	3.00
74121	1	1.50	1.50
AM9511	1	210.00	210.00
8T97	1	.93	.93
16 Pin Socket ST	6	.51	3.06
14 Pin Socket ST	13	.21	2.73
20 Pin Socket ST	5	.32.	1.60
24 Pin Socket ST	3	.91	2.73
PC Board	1	2.00	2.00
Artwork	-	10.00	10.00
Manufacture	-	5.00	5.00
TOTAL			$278.00

PROM BOARD	QTY	PRICE	TOTAL
Switch Pak	1	$ 2.25	$ 2.25
DM8160	1	2.00	2.00
74LS138	1	.72	.72
8T97	2	.93	1.86
DP8304/74LS245	2	1.50	3.00
7404	1	1.01	1.01
7432	1	.26	.26
7402	1	1.25	1.25
7474	1	1.37	1.37
2716	16*	45.00	720.00
Resistors (10K)	10	.03	.30
Capacitors (By Pass)	18	.37	6.66
Artwork	-	10.00	10.00
PC Board	1	2.00	2.00
Manufacture	-	5.00	5.00
16 Pin Socket ST	4	.51	2.04
14 Pin Socket ST	4	.21	.84
20 Pin Socket ST	2	.32	.64
24 Pin Socket ST	16	.91	14.56
TOTAL			$775.76

* Fully Populated

RAM BOARD	QTY	PRICE	TOTAL
Switch Pak	1	$ 2.25	$ 2.25
DM8160	1	2.00	2.00
74LS138	1	.72	.72
8T97	2	.93	1.86
DP8304/74LS245	2	1.50	3.00
7404	1	1.01	1.01
7432	1	.26	.26
7402	1	1.25	1.25
7474	1	1.37	1.37
4118-2	16*	28.00	448.00
Resistors (10K)	10	.03	.30
Capacitors (By Pass)	18	.37	6.66
Artwork	-	10.00	10.00
PC Board	1	2.00	2.00
Manufacture	-	5.00	5.00
16 Pin Socket ST	4	.51	2.04
14 Pin Socket ST	4	.21	.84
20 Pin Socket ST	2	.32	.64
24 Pin Socket ST	16	.91	14.56
TOTAL			$503.76

* Fully Populated

PARALLEL INPUT BOARD	QTY	PRICE	TOTAL
74LS138	2	$ .72	$ 1.44
81LS95	16	1.44	23.04
7404	1	1.01	1.01
8282	2	8.00	16.00
DM8160	1	2.00	2.00
Switch DIP	1	2.25	2.25
16 Pin Socket ww	8	.84	6.72
16 Pin Socket ST	3	.51	1.53
14 Pin Socket ST	1	.21	.21
20 Pin Socket ST	18	.32	5.76
Capacitor (.1,.01)	18	.37	6.66
Resistors (10K)	5	.03	.15
Artwork	-	10.00	10.00
PC Board	1	2.00	2.00
Manufacture	-	5.00	5.00
TOTAL			$ 83.77

PARALLEL OUTPUT BOARD	QTY	PRICE	TOTAL
Switch Pak	1	$ 2.25	$ 2.25
DM8160	1	2.00	2.00
74LS138	2	.72	1.44
Resistor (10K)	5	.03	.15
8282	18	8.00	144.00
16 Pin Socket WW	8	.84	6.72
16 Pin Socket ST	3	.51	1.53
20 Pin Socket ST	18	.32	5.76
Capacitors (By Pass)	18	.37	6.66
Artwork	-	10.00	10.00
PC Board	1	2.00	2.00
Manufacture	-	5.00	5.00
TOTAL			$187.51

DISCRETE I/O BOARD	QTY	PRICE	TOTAL
16 Pin WW Socket	8	$ .84	$ 6.72
2N2222	32	.18	5.76
7407	6	.30	1.80
Resistors (10K)	32	.03	.96
Resistors (1K)	32	.03	.96
Dual N Channel MOSFET	16	2.00	32.00
Artwork	-	10.00	10.00
PC Board	1	2.00	2.00
Manufacture	-	5.00	5.00
TOTAL BOARD			$ 65.20

DISK CONTROLLER/ DIRECT MEMORY ACCESS	QTY	PRICE	TOTAL
7404	7	$ 1.01	$ 7.07
7432	1	.26	.26
7402	2	1.25	2.50
74121	4	1.50	6.00
8257	1	26.50	26.50
74LS373	1	2.00	2.00
DP8304	5	1.50	7.50
81LS97	1	1.44	1.44
74LS138	3	.72	2.16
7474	1	1.37	1.37
7417	1	1.53	1.53
FD1791B	1	49.95	49.95
CD4046	1	1.79	1.79
7400	1	1.33	1.33
74175	1	.79	.79
40 Pin Bus Connector	3	6.05	18.15
1 MHz XSTAL	1	14.87	14.87
Capacitors	6	.37	2.22
Resistors	25	.03	.75
Potentrometer 25K	2	1.00	2.00
Potentrometer 5K	2	.90	1.80
Diodes	10	.06	.60
Capacitors (220 μf)	1	1.79	1.79
Artwork	-	10.00	10.00

PC Board	1	2.00	2.00
Manufacture	-	5.00	5.00
14 Pin Socket ST	18	.21	3.78
16 Pin Socket ST	4	.51	2.04
20 Pin Socket ST	7	.32	2.24
40 Pin Socket ST	2	1.39	2.78
TOTAL			$182.21

HYBRID INTERFACE/ SERIAL I/O/TIMER BOARD	QTY	PRICE	TOTAL
40 Pin Edge Connector	2	$ 6.05	$ 12.10
8253	1	25.00	25.00
8251	1	13.20	13.20
7404	4	1.01	4.01
7490	3	2.78	8.34
74163	1	.57	.57
MM5307	1	15.00	15.00
10 MHz XSTAL	1	6.31	6.31
8.29 MHz XSTAL	1	10.25	10.25
DM8160	2	2.00	4.00
7408	1	.31	.31
7400	1	1.33	1.33
74LS138	1	.72	.72
81LS95	2	1.44	2.88
DP8304	2	1.50	3.00
14 Pin ST	12	.21	2.52
16 Pin ST	2	.51	1.02
28 Pin ST	1	1.10	1.10
24 Pin ST	1	.91	.91
20 Pin ST	4	.32	1.28
Artwork	-	10.00	10.00
PC Board	1	2.00	2.00
Manufacture	-	5.00	5.00
TOTAL			$130.85

D/A BOARD	QTY	PRICE	TOTAL
74LS138	1	$ .72	$ .72
74LS174	4	.67	2.68
AD565	2	35.00	70.00
AD171J	2	83.53	167.06
100K Pot	2	.93	1.86
10K Pot	2	.96	1.92
Resistors (2.2K,50Ω)	6	.03	.18
Capacitors (15μfd)	4	.28	1.12
Artwork	-	10.00	10.00
Manufacture	-	5.00	5.00
PC Board	1	2.00	2.00
TOTAL			$262.54

A/D CONTROLLER BOARD	QTY	PRICE	TOTAL
81LS96	2	$ 1.44	$ 2.88
7489	4	3.25	13.00
74163	2	.57	1.14
74LS138	2	.72	1.44
74S157	1	.53	.53
74123	1	2.25	2.25
74151	1	1.25	1.25
7404	1	1.01	1.01
7400	1	1.33	1.33
16 Pin WW Socket	2	.84	1.68
16 Pin Socket ST	11	.51	5.61
14 Pin Socket ST	3	.21	.63
20 Pin Socket ST	2	.32	.64
PC Board	1	2.00	2.00
Artwork	-	10.00	10.00
Manufacture	-	5.00	5.00
Capacitors (	9	.37	3.33
Resistors (Misc)	17	.03	.51
TOTAL			$ 54.20

SERIAL I/O INTERFACE	QTY	PRICE	TOTAL
Banana Connector	11	$ .15	$ 1.65
4N33	2	1.87	3.74
1N914	2	.06	.12
Resistor	6	.03	.18
7406	1	1.78	1.78
75188	1	1.07	1.07
75189	1	1.07	1.07
Artwork	-	2.00	2.00
Manufacture	-	2.00	2.00
PC Board	1	2.00	2.00
TOTAL			$ 15.61

APPENDIX B

EDUCATIONAL GOALS AND PARTICIPANTS

At the Air Force Academy our goals extended beyond the technical goals given on pages 2 and 3 to include certain educational goals. The Department of Electrical Engineering desired to provide those rare and exceptionally outstanding students a challenge beyond the mere pages of a text book and bordering on actual design as it might be encountered in the real engineering world. Over the course of this project many cadets have incidently and directly become involved with the computer system, providing them an insight into the world of design and an experience not normally available to the typical undergraduate student. Wherever possible, concepts originally taught in Electrical Engineering courses were expanded for application in this system.

The following list details areas of responsibility within the project.

SUBSYSTEM	DESIGNER	CHAPTER
Bus System and Power Distribution	Capt J. Pollard	I
Front Panel/Single Step Control	Lt J. McCormack	II
Front Panel Controller	Capt J. Pollard	III
CPU/Interrupt Control/DMA Control	Lt J. McCormack	IV
	Capt J. Pollard	
EPROM/RAM Memory	Lt M. Baumgartner	V
Parallel Input Ports	Lt W. Davidson	VI
	Lt A. Bonutti	
Parallel Output Ports	Lt W. Davidson	VII
	Lt A. Bonutti	

AM9511 Arithmetic Processor	Lt T. Mundelein	VIII
	Capt J. Pollard	
Hybrid Interface/Serial I/O/Timer	Capt J. Pollard	IX
RS232/20 ma Loop Interface	Capt J. Pollard	IX
Hybrid Subsystem (A/D and D/A)	C1C N. Catone	X
	Capt J. Pollard	
Special 28 Volts Relay I/O	Lt W. Davidson	XI
	Lt A. Bonutti	
Floppy Disk Controller	Lt M. Baumgartner	XII
	Lt D. McGrath	
Direct Memory Access Control	Lt M. Baumgartner	XIII
System Peripheral Devices	Capt J. Pollard	XIV
System Software	Capt J. Pollard	VOL II
	C1C G. Rosenberger	
	C1C P. Fitzjarrell	
System Cost Analysis	Capt J. Pollard	APPENDIX A

In addition to those personnel directly associated with particular system modules Captain A.R. Klayton and Captain F. Cruger of the Computer Systems Laboratory (DFEE) provided moral and psychological support over the duration of the project lending to the successful project completion.

LME